education systems

EA180

REFERENCE AND MAINTENANCE MANUAL

EAI 180 COMPUTER

OPERATOR'S REFERENCE AND MAINTENANCE MANUAL

EAI-ELECTRONIC ASSOCIATES PTY. LTD. PRINTED IN AUSTRALIA. JULY 72
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NOTICE

When ordering or enquiring about spare parts and replacement units for your 180 Computer, we request that you use the following procedure.

1. Supply the Drawing Number and Circuit Reference which is listed in the parts listing at the back of this manual and the model and serial numbers of the computer. Without this information we cannot process your request.

2. If the item is a mechanical part or assembly which does not have the above reference, please supply a full description and the model and serial numbers of the computer.
   If possible, include the purchase order or the EAI project number under which the equipment was originally purchased.

Your co-operation in supplying the required information will speed the processing of your requests and aid in assuring that the correct items are supplied.

It is the policy of EAI-Electronic Associates Pty. Limited to supply equipment patterned as closely as possible to the requirements of the individual customer. This is accomplished, without incurring the prohibitive costs of custom design, by substituting new components, modifying standard components, etc., wherever necessary to expedite conformance with requirements. As a result, this instruction manual, which has been written to cover standard equipment, may not entirely cover modified equipment. It is felt, however, that a technically qualified person will find the manual a fully adequate guide in understanding, operating, and maintaining the equipment supplied.

EAI-Electronic Associates Pty. Limited reserves the right to make changes in design, or to make additions to or improvements in its product without imposing any obligation upon itself to instal them on products previously manufactured.

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CHAPTER 1

1.1 INTRODUCTION

Many problems encountered in scientific, engineering and educational work involve mathematical equations or sets of equations whose solution in most cases is difficult or practically impossible to obtain by the classical approach to equation solution. The EAI-180 Analog Computer provides the technical worker with a general purpose computer which permits the rapid solution of linear or non-linear equations.

Although the analog machine is correctly termed a computer, it does not perform its computations by serial calculations as does the desk calculator or digital computer. Instead it performs the required mathematical operations in a parallel manner on continuous variables. In the EAI-180, as in most modern analog computers, the continuous variables are direct current voltages. The electronic analog computer makes it possible to build an electrical model of a physical system, where the voltages on the computer represent the dependent variables of the physical system. Except for a constant of proportionality, or scale factor, each voltage will behave with time in a manner similar to the physical system variable. Thus, if the vertical position of the center of gravity of an automobile oscillates with time during a disturbance, then the voltage representing the height of the center of gravity above the surface will also oscillate; if the temperature of the coolant at the exhaust port of a condenser rises exponentially to a steady value, then so will the voltage representing it on the computer.

It can be said that the actual system and the electrical model are analogous in that the variables which demonstrate their characteristics are described by relations which are mathematically equivalent. The actual system has thus been simulated because of the similarity of operation of the electrical model and the physical system. This capability of the analog computer is of great value in performing scientific research or egineering design calculations because it permits an insight into the relationship between the mathematical equations and the response of the physical system. Once the electrical model is completed, well-controlled experiments can be performed

quickly, inexpensively, and with great flexibility to predict the behaviour of the primary physical system.

Although the analog computer utilizes electronic components in its operation, it is not essential that the user have an extensive knowledge of electrical circuits. The EAI-180 is basically a set of mathematical building blocks, each able to perform specific mathematical operations on direct voltages and capable of being easily interconnected. By appropriately interconnecting these building blocks, an electrical model is produced in which the voltages at the outputs of the blocks obey the relations given in the mathematical description of a physical problem.

Since our interest is frequently in the dynamic behaviour of physical systems, the mathematical equations are usually differential equations having time as the independent variable. In order to solve such equations, the standard components of the computer must perform the following operations: inversion, algebraic summation, integration with respect to time, multiplication and division, and function generation.

The sequence of steps for constructing a dynamic model on an analog computer requires first a mathematical description of the physical system, usually in equation form. From this description the operator derives the information necessary to set up a computer program for interconnecting the computing components and determines the required initial conditions and forcing functions. The computing components are interconnected with wires called patch cords. The input and output terminations of the computing components are brought out to a patch bay panel. The problem is placed on the computer by patching and adjusting the problem parameters to the value of the first case to be investigated. Selected voltages are applied to various components in the form of inputs or initial conditions. These voltages are derived from a precise reference voltage.

Once the computing elements have been patched, adjusted, and energised, the computer is switched into the operate mode. The voltages on the computer change with time in accordance with the equations that govern the physical system variables. The behaviour of the computer model is viewed through an output device such as an X-Y plotter, oscilloscope,

strip-chart recorder, or digital voltmeter.

The EAI-180 Operator's Reference and Maintenance Handbook has been prepared to serve as a working guide to the analog programmer or computer operator. The information contained presupposes a knowledge of the analog computer, its basic principles of operation, and programming procedures. (Instructional information in these areas can be obtained from "Basics of Analog Computer Programming" by the EAI Education and Training Group). Readers interested in more detailed circuit information are referred to the Maintenance section of the manual.

1.2 GENERAL DESCRIPTION

The EAI-180 (figure 1) is a general purpose analog computer composed of solid-state computing components. The EAI-180 is compact in size and is able to operate with stability and precision in a normal office or classroom environment. Reliable, with simplicity in functional design, the EAI-180 is easy to use and can be powerful aid to the individual engineer or student in the rapid solution of scientific and engineering problems.

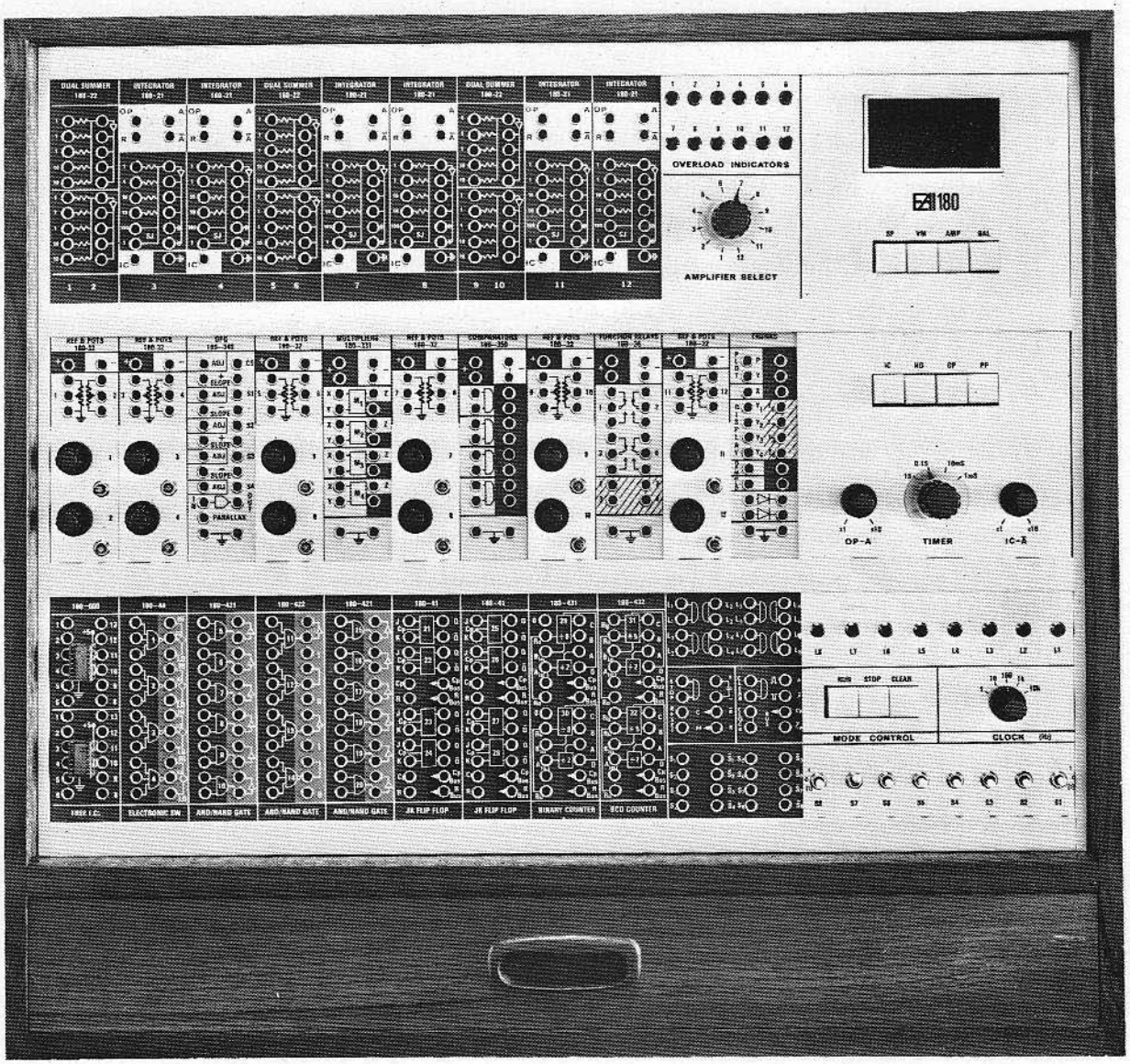
Table 1 (page 25) lists the currently available computing components and accessories for the EAI-180. The EAI-180 utilizes a building block concept, in which individual computing components may be easily inter-connected to solve the required equations by forming electronic models analogous to the system under study. Each building block, either individually or in combination with others, is capable of performing one or more mathematical operations. The computing components in the EAI-180 occupy the area to the left of the control panel area. This area is divided into three rows; the top row contains linear components, summers and integrators; the middle row houses the non-linear components and potentio-meters; the bottom row contains Logic components. The computing components are constructed on plug-in cards, and the front of each computing component consists of a color-coded plastic patching overlay that contains the input and output termination for the unit. The computing components are inter-connected by placing patch cords or bottle plugs between the appropriate input and output terminations. The patching layout

of the EAI-180 has been designed to be compatible with larger EAI computors so that experience gained on the EAI-180 can be readily transferred to larger machines.

To the right of the patching area is the monitoring and control area which contains controls and components that permit the control of the computer and its modes of operation and the measurement of problem variables.

The EAI-180 is completely tested and calibrated at the time of manufacture and is shipped with all components in place. After performing the preliminary check-out procedure outlined in the EAI-180 Maintenance Manual, the computer is ready for operation.

It should be noted that the low voltage levels used in the EAI-180 eliminate any shock hazard to the operator when patching components with the computer turned on. Current-limiting circuits protect the reference supplies, and amplifier outputs from damage during short-term overloading if they are inadvertently patched to ground or to each other.



THE EAI -180 ANALOG-HYBRID COMPUTER

CHAPTER 2

OPERATING PROCEDURES

2.1 INITIAL SET UP PROCEDURES

In order to ensure that the equipment will function correctly, it is advisable that the following initial set up procedure be followed before the equipment is switched on.

2.1.1 Rating

Check that the equipment is correctly rated for either 240V, 50HZ or 110V-60HZ operation. This information is displayed on the rating plate located on the back of the computer.

2.1.2 Integrator Mode

Check that all integrators have dual bottle plugs connecting control signals A and $\overline{A}$ to OP & R busses respectively.

2.1.3 Integrator Feedback

Check that all integrators have a 1 MF capacitor connected in the Feedback loop. A single bottle plug may be used for this purpose, connecting to the input/output positions indicated by '1' (the capacitor positions are 1 & 100 volts per second respectively).

2.1.4 Summer Feedback

Check that all summers have a 1M ohm resistor connected in the feedback loop. A single bottle plug may be used for this purpose, connecting to the input/output positions indicated by '1' (the positions 1 & 10 refer to amplifier gain).

2.1.5 Control Switches and Push Buttons

Check that all rotary switches and push buttons are in the following positions:

(a) Meter Function Push-button — VM
(b) Mode Control Push-button — IC
(c) Digital Mode Control Push-button — STOP
(d) Timer switch — 1 second
(e) OP-$\overline{A}$ and IC-A controls — x1

2.1.6 Slaving Plug

Check that a dummy slaving plug is fitted to the slaving output socket at the back of the computer. If two computers are to be slaved together, then a slaving cable should be connected between the two slaving output sockets.

2.1.7 Switch ON

Switch power ON and allow 10 mihutes warm-up. Note for safety reasons the power switch is located on the back of the unit so that no large voltages are connected to the front panel.

2.1.8 Reference Supplies

Check and adjust if necessary both +ve and —ve references (+1.000 and —1.000 machine units). Reference adjustments are located at the back of the computer. This is done by connecting first the positive then the negative reference to the DPM input on the TRUNK panel.

The Digital Panel Meter should be checked with a 4½ digit DVM approximately every 6 months — no zero adjustment is necessary and both +ve and —ve fullscale adjustments are performed with one front panel adjustment (see Maintenance Section).

2.1.9 Amplifier Balance

Check amplifier balance by carrying out the following procedure.

a) Set Meter Function Switch to BAL. This operation automatically operates all amplifier balance relays. Amplifier output is indicated by the DPM.

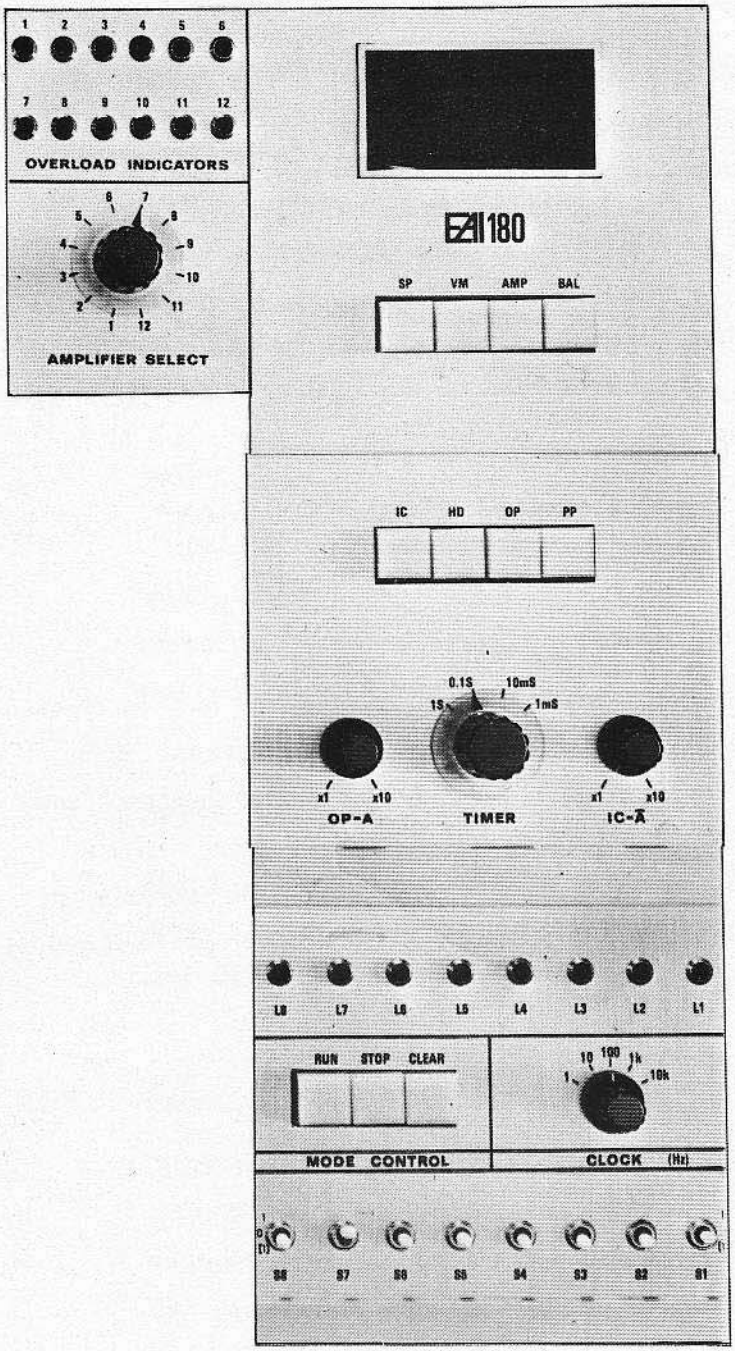
b) Select each amplifier in turn and balance if necessary by inserting a fine pointed srewdriver into the summing Junction Terminal. The amplifiers may be regarded as being correctly balanced of the DPM gives a .000± 1 digit reading.

c) When complete set Meter Function P/B to AMP.

2.1.10 Digital Panel

If required the clock and mode control operation may be checked by connecting Cp, R & $\overline{R}$ to separate lamp indicators. With Clock Frequency Selector in 1 HZ position, clock operation will be evident if Digital Mode control P/B are in either RUN or CLEAR modes. Conditions of R & $\overline{R}$ signals will change when Digital mode control P/B is placed in either STOP or RUN modes.

The EAI-180 is now ready for operation.



READOUT AND METER CONTROL

DISPLAY MODE CONTROL

DIGITAL CONTROL

CONTROL AREAS OF EAI-180 COMPUTER

FIG: 2

2.2 OPERATING INSTRUCTIONS

The EAI-180 Analog/Hybrid small scale computing system, has 3 MAJOR control areas located on the RH side of the patching area. These are illustrated in fig. 2 and are —

2.2.1 READOUT and METER CONTROL

2.2.2 DISPLAY and MODE CONTROL

2.2.3 DIGITAL CONTROL

The function of these control areas will be discussed next. Note that all push buttons are shown in box ☐ and sockets in brackets ( ).

2.2.1 Readout and Meter Control

This control area allows the selection of amplifier outputs, meter functions and indicates if any amplifiers exceed limits.

2.2.1.1 METER FUNCTION SWITCH is a 4 position Push-button switch mounted below the meter and is used to determine meter functions as set out below.

a) [P.B.] When POT BUS position is selected, any potentiometer setting can be read directly by depressing the appropriate potentiometer select switch. This allows quick setting of potentiometers to better than ± .1%.

b) [VM] When the VM position is selected, any computer or external voltage in the range ±20 volts can be read by applying this voltage to the (DPM) socket on the TRUNKS panel.

2.2.1.1 c) [AMP] This position enables an amplifier output to be displayed on the output meter by selecting the appropriate amplifier on the AMPLIFIER SELECT, 12 position switch.

The selected amplifier output is simultaneously applied to the (AMP) socket located on the trunk panel.

d) [BAL] The selection of this position actuates all balancing relays.

2.2.1.2 AMPLIFIER SELECT SWITCH

This 12 position switch is used to select the amplifier outputs for presentation to the meter or to the external readout equipment which has been connected to (AMP) socket located on the TRUNK panel.

The (AMP) socket is connected directly to the AMPLIFIER SELECT switch and is not affected by the position of the METER FUNCTION Switch.

2.2.1.3 OVERLOAD INDICATORS

When an amplifier output exceeds a voltage of approximately 10.5 to 11V, the overload INDICATORS will light and simultaneously ground the overload socket (OVL) on the TRUNKS panel. The overload light will remain on until the cause of overload is removed.

2.2.1.4 DIGITAL PANEL METER

This 3½ Digit instrument is used to monitor all computer variables. This unit requires calibration approximately every 6 months and features a unique automatic "zeroing" circuit.

NOTE the DPM accuracy is an order higher than the overall accuracy of the system, hence do not carry out unnecessary adjustments on the DPM.

2.2.2 Display and Mode Control

The Display and Mode Control area shown in fig. 2 provides a means of controlling the solution of problems set up on the analog computers and of conveniently connecting these solutions to display devices.

2.2.2.1 Mode Control

The computer can essentially be placed into 3 modes as follows —

a) IC

In the initial condition mode, the output voltage of the integrators are set to the values required by the initial conditions of the problem.

b) HD

In the hold mode, all inputs to the integrators are removed and all variables are held at a constant value.

c) OP

In the operate mode, the integrators accept inputs and integration and problem solution takes place.

Integrators can be mode controlled by means of signals (A) & ($\overline{A}$) which may be connected to the integrator mode control inputs (OP) and (R). The control signals can assume the values listed in the truth table over leaf.

MODE	A	$\overline{A}$
Not Allowed	0	0
Operate OP	0	1
Initial Condition IC	1	0
Hold HD	1	1

NOTE: 0 = 0 ± 0.25 volts (or connected to ground)
1 = 3 ± 1 volt (or open circuit).

There are 4 methods of controlling computer modes and these are discussed below.

MANUAL OPERATION

In this mode of operation, all integrators connected to the control busses (A) & ($\overline{A}$) can be controlled by using the 3 push buttons marked IC , HD and OP .

Whenever a push button is depressed, it will be illuminated to indicate the mode which has been entered.

REPETITIVE OPERATION PP

In this mode an automatic Timer produces repetitive control signals (A) & ($\overline{A}$) which, if connected to the integrator mode controls (OP) & (R) will repetitively set to IC and OPERATE all integrators thus connected. The waveforms produced by the Timer are shown in fig. 3.

The basic Timer period can be adjusted over the ranges shown in the table below –

TIMER PERIOD	OP TIME (A)	IC TIME ($\overline{A}$)
1 sec	1 sec to 10 sec	.1 sec to 1 sec
.1 sec	.1 sec to 1 sec	.01 sec to .1 sec
10 ms	10 ms to 100 ms	1 ms to 10 ms
1 ms	1 ms to 10 ms	.1 ms to 1 ms

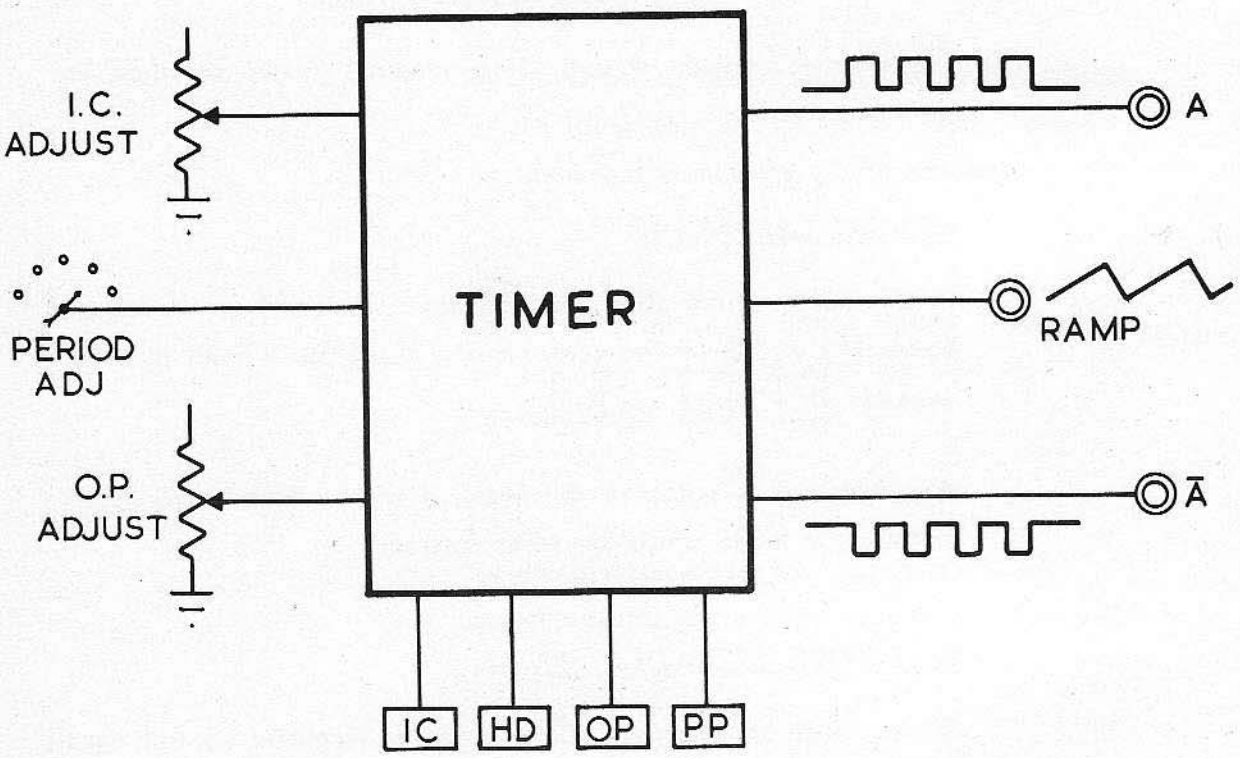


FIG: 3

MODE CONTROL & TIMER WAVEFORMS

The Timer period is controlled by the centrally located 4 position switch.

The (OP) and (IC) times can be independently adjusted by the two potentiometer controls over a range of 1:10. The Timer generator also produces a linear ramp which may be used as a time base for external display equipment, this is available on the TRUNKS panel.

Note that during manual operation, the linear ramp will still be produced when the operate push button is depressed. However, the ramp output will saturate if the computer is left in the operate mode for too long.

SLAVED MODE

TWO EAI-180 Computers can be slaved together to simulate larger problems. Slaving is carried out by removing the Dummy slaving plugs and linking the two computers with a slaving cable.

This procedure effectively transfers operation of the mode control of both computers, to the unit to which the RED coded connector of the slaving cable is connected.

The mode control of the slave is still operative and may be used to control integrators by directly patching from the (A) and ($\overline{A}$) sockets on the TRUNKS panel to the individual integrator (OP) and (R) sockets.

Amplifier readout selection and metering still remains under the control of each computer.

EXTERNAL DIGITAL CONTROL

By the connection of appropriate control signals to the OP and R terminals, the integrator may be controlled by external digital signals.

NOTE: The integrators present approximately one ½ of a DTL/TTL unit load and the following input logic levels may be used without damaging the circuitry.

Logic 1 = + 2.0 volts to + 15 volts or O/C

Logic 0 = 0 to + 1 volts or S/C.

2.2.2.2 Trunks and Display Panel

All common control signal and display device terminations are brought out as sockets on the TRUNK panel.

Plotter Inputs (PLOT)

(P) X-Y Plotter pen control.
Depending on the type of X-Y plotter, application of the appropriate mode control signal (A or $\overline{A}$) will ensure pen is in the UP position when the computer is in the IC mode.

(X) (Y) Plotter inputs, voltages connected to these sockets will cause the X-Y plotter arm to move.

This socket is also connected to the X input of the CRT display.

CRT Display scope (DISPLAY)

(Y1)
(Y2)
(Y3)
(Y4)

4 sockets labelled Y1, Y2, Y3, Y4 are provided for the connection of 4, Y (vertical) signals to the CRT display scope.

DIGITAL PANEL METER

(DPM) Provided METER FUNCTION switch is in position VM, a voltage connected to this socket will be displayed on the Digital panel meter.
(AMP) Output of AMPLIFIER SELECTOR.

SYSTEM HOLD

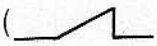
(HLD) Applying a logic zero (short to ground) signal to this socket will place all integrators into the hold mode.

(OVL) Overload signal generates if an overload condition exists.

NOTE: If (OVL) is connected to (HDL), the system "freezes" if an overload occurs.

TRUNKS

(T1) (T2) (T3) (T4) These sockets are connected to a connector at the back of the computer and are available for trunking signals to and from the computer.

() Ramp output. This socket provides a ramp output produced by the system timer. This signal can be used as an X signal to X-Y recorders or CRT display.

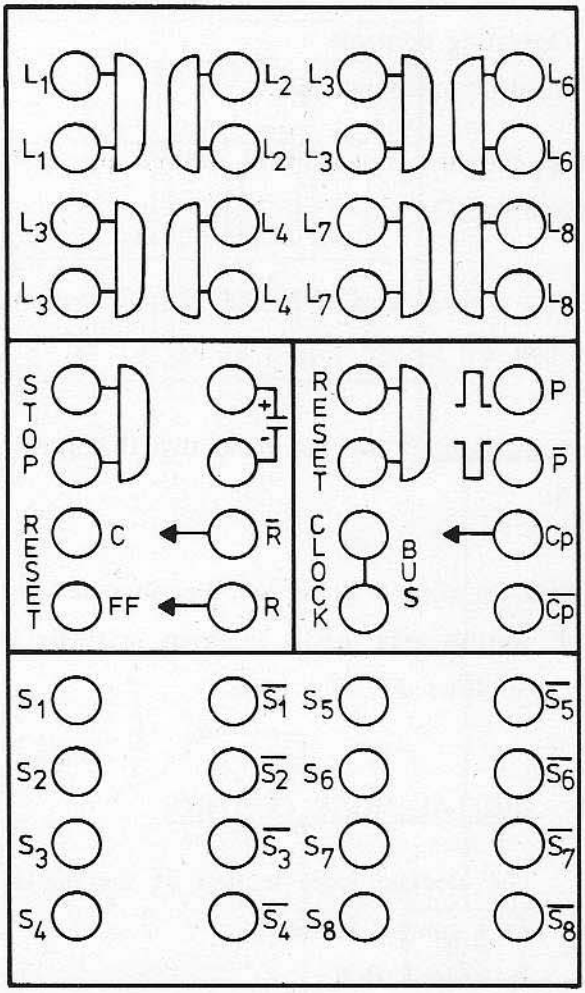


FIG: 4

LOGIC CONTROL PATCHING AREA

2.2.3 Digital Control

The following descriptions apply to computers fitted with a digital panel for basic digital and hybrid problems.

The digital control area is divided into two sections:

a) Operating controls
b) Control patching area

Note that the operating control outputs are available on the control patching area.

The digital control area is further sub-divided into 4 functional areas which are clearly shown in fig. 4.

A block diagram of the complete digital control circuitry is shown in fig. 5.

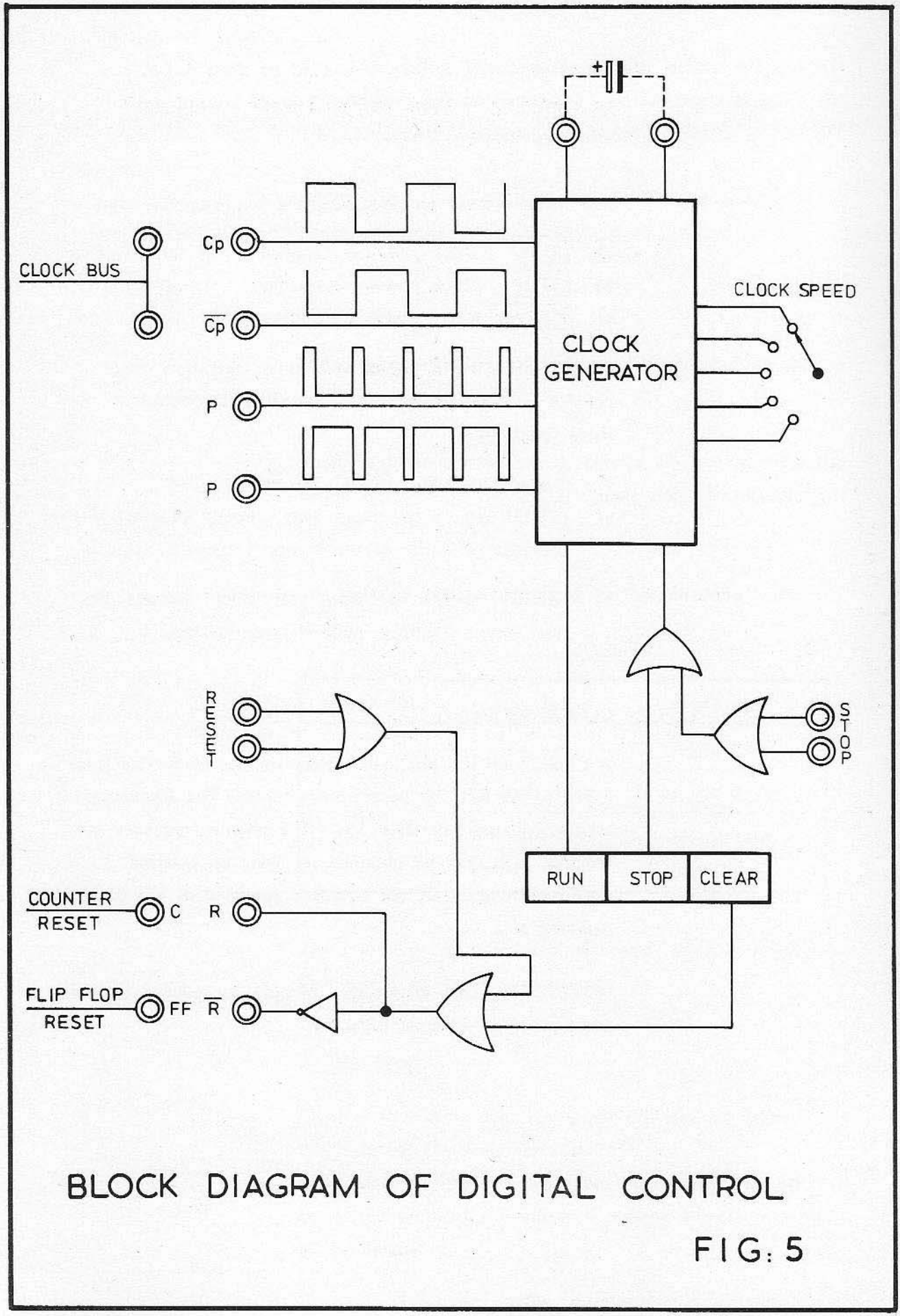
These separate control areas will be discussed next.
Note, all control area inputs represent a single DTL load and all outputs will drive 20 DTL loads.

2.2.3.1 DIGITAL MODE CONTROL

The clocked logic section of the digital panel is supplied with control busses:

a) Clock Bus
b) Counter Reset Bus
c) Flip Flop Reset Bus

to which a clock source and reset signals should be applied. In normal operation a double bottle plug would be inserted to join ($\overline{R}$) to counter Reset Bus (C), (R) to (FF) reset bus and a single bottle plug from (Cp) source to the CLOCK bus.



BLOCK DIAGRAM OF DIGITAL CONTROL

FIG: 5

Any logic which is then connected to these busses can be controlled by operating the 3 mode control push button switches.

The mode control switches have the following functions —

a) RUN Clock pulses are applied to CP bus.
b) STOP Clock pulses are disabled
c) CLEAR Reset Busses are activated.

As an alternative to the above manual operation, mode control can be performed by external logic control of these functions.

For this purpose two control gates are provided:

a) (STOP) gate; a two input gate which stops clock operation if either of the inputs is taken to logic 0.

b) (RESET) gate; a two input gate which operates the reset busses if either input is taken to logic 0.

2.2.3.2 CLOCK SOURCE

A Clock source is provided which supplies frquencies from 1 HZ to 10 KHZ in decade increments. The frequency accuracy is approximately 5%. If a precise frequency is required, this may be obtained by using an external capacitor mounted at the terminals provided in the control patching area.

NOTE: The clock frequency can only be reduced by the addition of an external capacitor.

The clock source also provides a pulse output (P) and ($\overline{P}$) which occurs whenever the clock changes level. The appropriate waveforms are shown in fig. 5.

NOTE: Only a single bottle plug should be used in connecting clock source to CLOCK Bus.

2.2.3.3 SWITCHES

Eight independent control switches are provided on the control panel.

These switches operate switch bounce elimination bistables whose outputs (S) and ($\overline{S}$) are made available on the control patching area.

The switches operate according to the following truth table.

Switch Setting	(S) Output	($\overline{S}$) Output
0	Logic 0	Logic 1
1	Logic 1	Logic 0
(1)	Momentary logic 1	Momentary logic 0

These switches may be used to operate logic in single shot mode, set binary values, etc.

2.2.3.4 INDICATORS

Eight gated independent lamps are provided to display the states of the logic variables.
Each lamp is driven by a 2 input AND gate. An un-connected terminal will act as if a logic 1 were presented at its input.

CHAPTER 3
COMPONENT DESCRIPTION

The active components of the EAI 180 are located on 3 panels —

(A) LINEAR PANEL
(B) NON LINEAR PANEL
(C) DIGITAL PANEL

3.1 LINEAR PANEL

The Linear panel as illustrated in fig. 6 contains the patching outlets for up to —

6 Integrators
3 Dual Summers.

The Procedures for balancing these amplifiers has been outlined in Chapter 1 and their characteristics will next be described.

3.1.1 Dual Summers

Both the front panel layout and schematic diagram of the Dual Summer is shown in fig. 7.

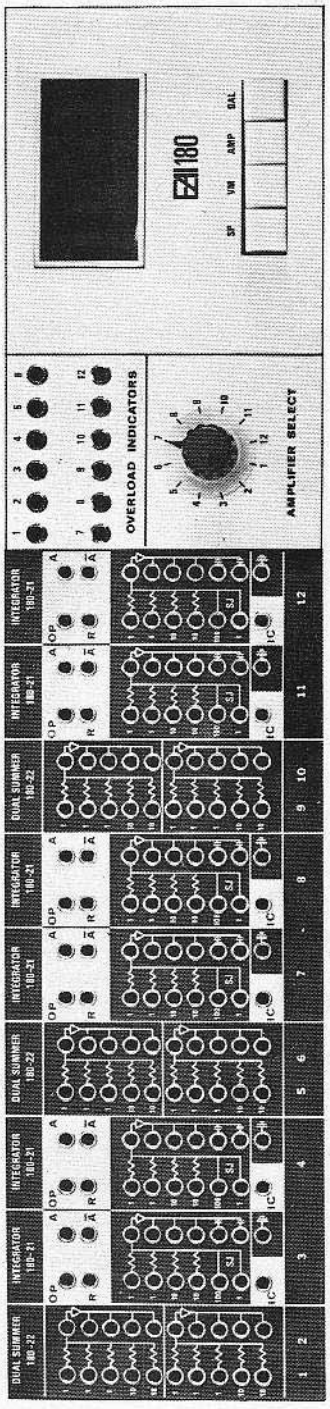
Each Summer consists of a high performance Fet-input operational amplifier and 5 computing resistors.

a) Three 1 M ohm Resistors (Gain 1)
b) Two 100K ohm Resistors (Gain 10).

These precision resistors are matched to 0.25%.

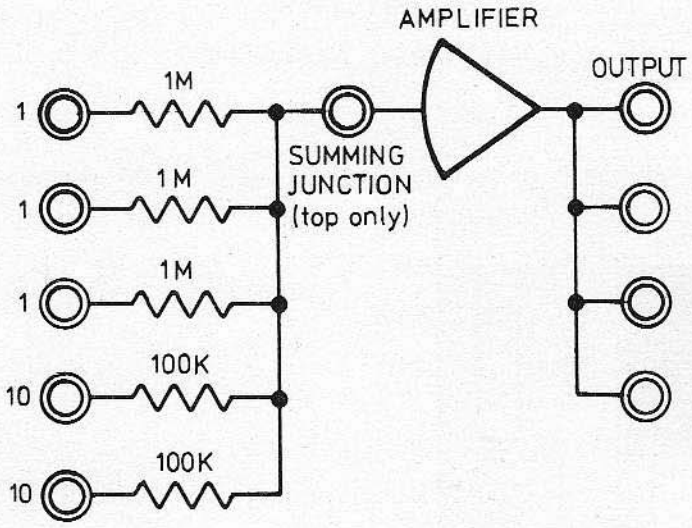
In operating the Summer an appropriate feedback resistor should always be connected otherwise an overload condition will result.

The computing resistors may be arranged in any gain configuration between .1 and 10. GAIN values outside these limits may result in some degradation of performance.



AMPLIFIER PANEL LAYOUT

FIG: 6



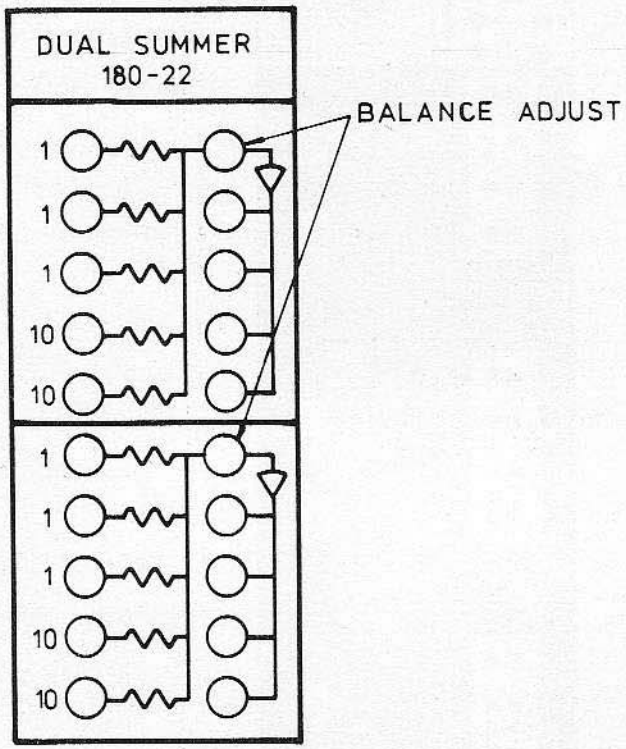
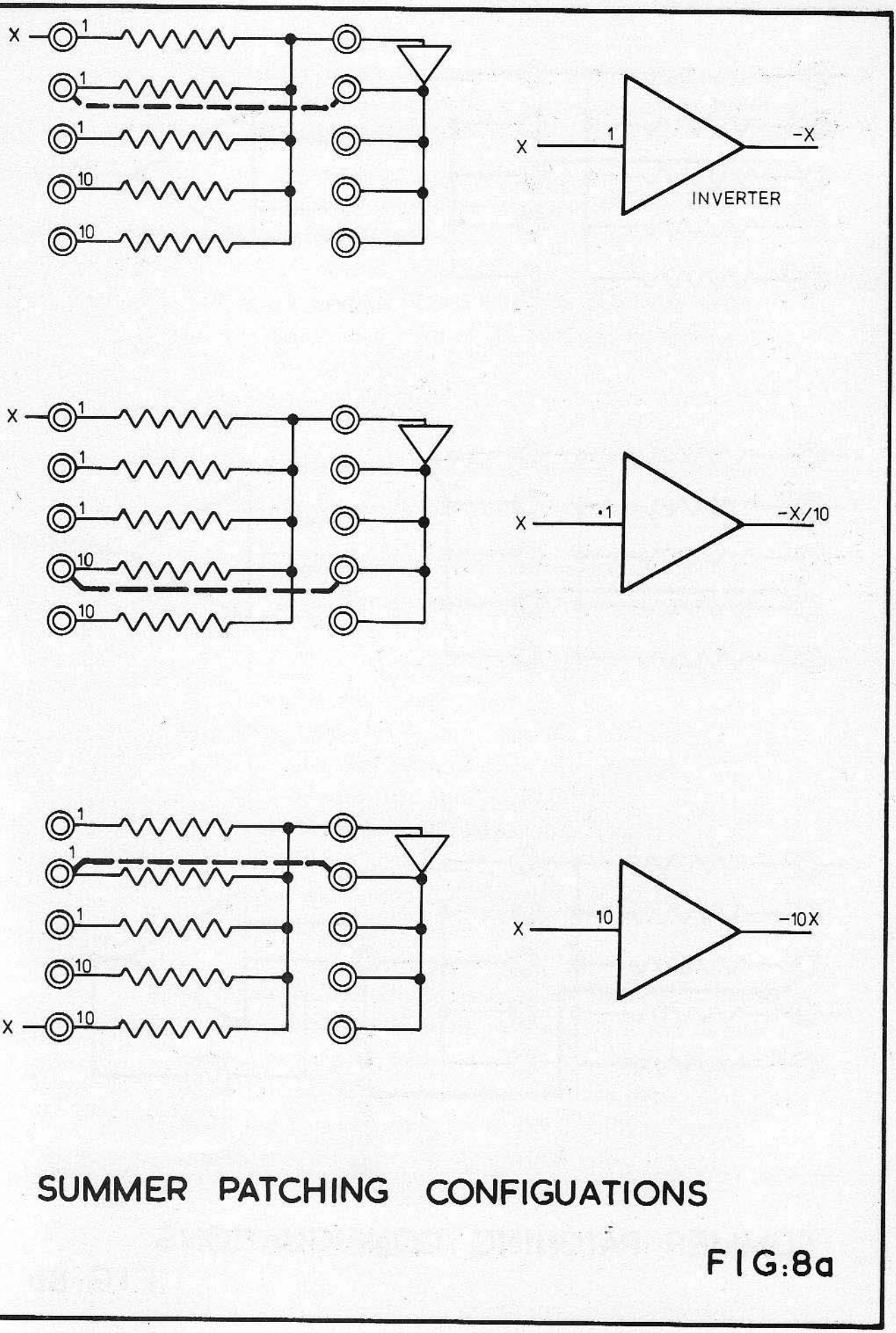
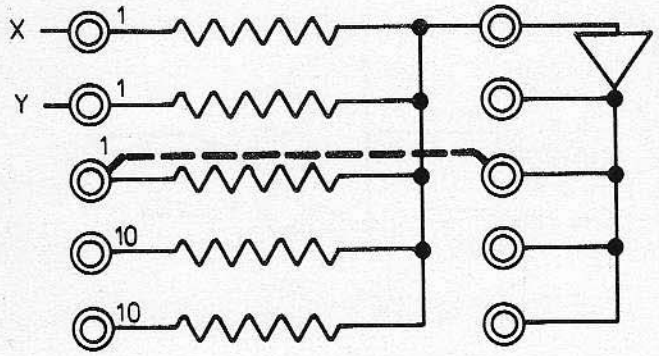


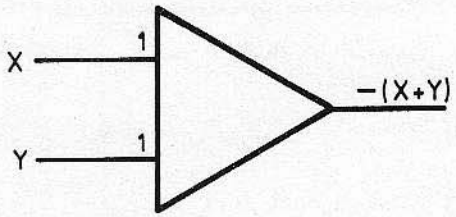
FIG: 7
DUAL SUMMER BLOCK DIAGRAM
AND FRONT PANEL

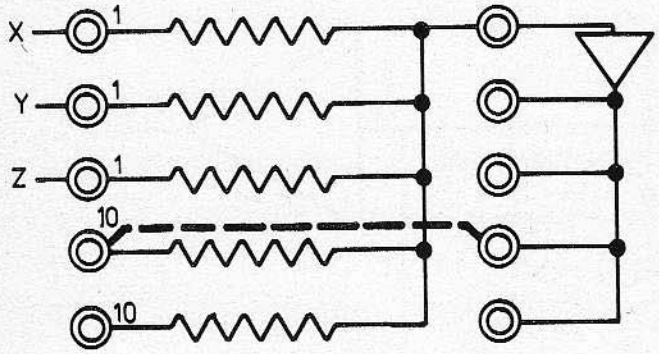


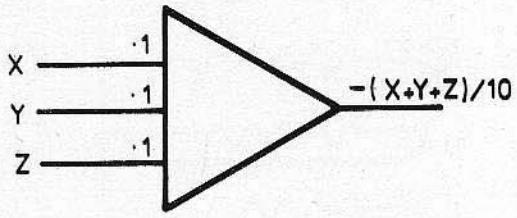
SUMMER PATCHING CONFIGUATIONS

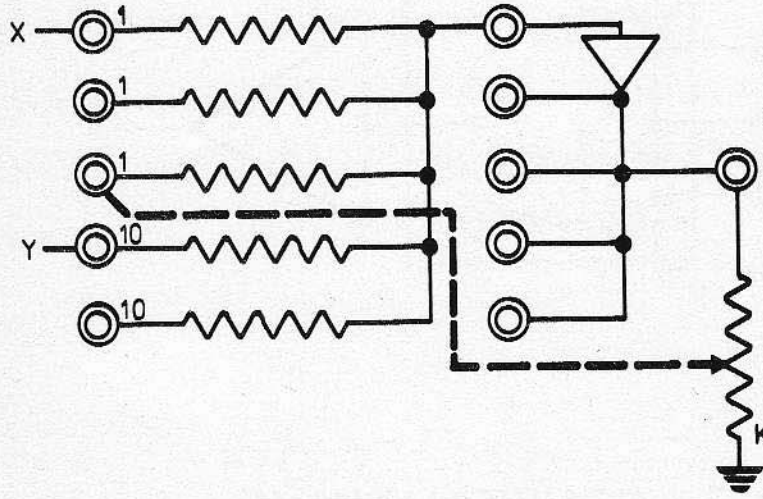
FIG:8a

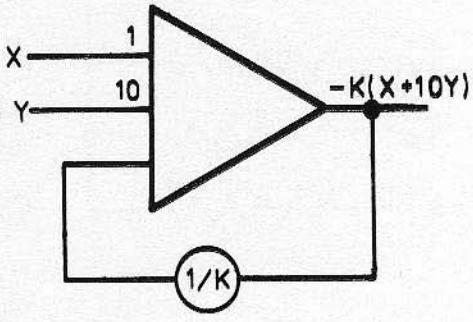












SUMMER PATCHING CONFIGUATIONS

FIG: 8b

The maximum output current capability of the operational amplifiers used is ± 5 MA; the amplifier is short circuit proof to ground or either reference supplies.

This output current rating places a limit on the number of potentiometers which may be driven.

Patching configurations — Figs. 8a and 8b show some of the patching configuration which can be used with the summer.

3.1.2 Integrators

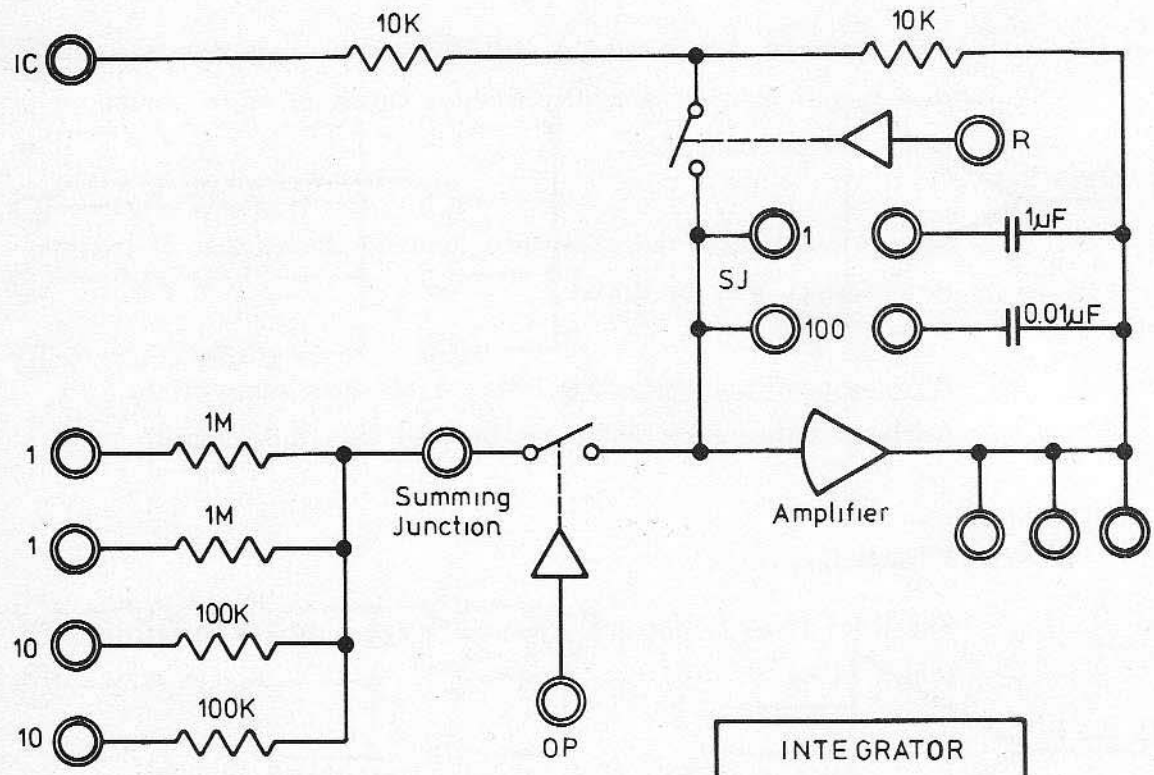
The front Panel layout and schematic diagram of the integrator is shown in fig. 9.

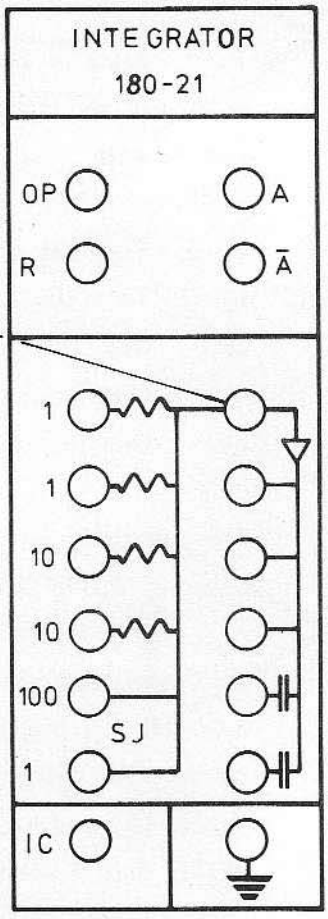
Each integrator consists of a Fet input operational amplifier, electronic mode control switches and the following computing components.

a) Two 1M ohm resistors (Gain 1)
b) Two 100K ohm resistors (Gain 10)
c) One 10K ohm initial condition input (Gain 1)
d) One 1 micro farad capacitor (Gain 1)
e) One .01 micro farad capacitor (Gain 100).

The resistors are matched to within .25% and the capacitors are accurate within 25%.

An appropriate feedback component should always be connected otherwise an overload condition will result. It is also advisable to connect the integrator mode control inputs to the mode control signals (A) and ($\overline{A}$) by using a double shorting plug.
NOTE that if mode control inputs (OP) and (R) are open circuited then integrator will be in HOLD mode.

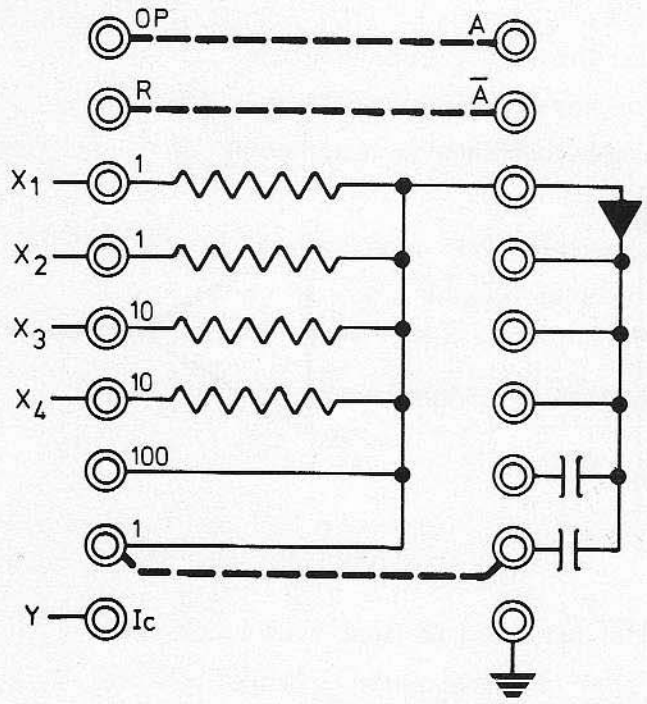


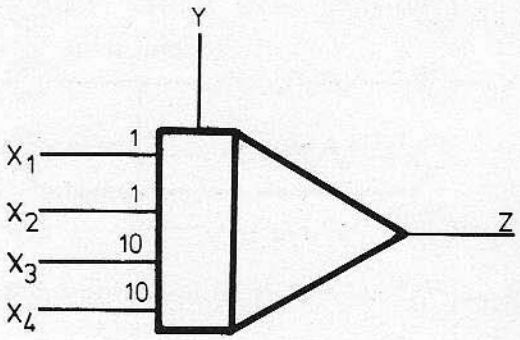


BALANCE ADJUSTMENT

OP	R	FUNCTION
0	0	NOT ALLOWED
0	1	COMPUTE
1	0	INITIAL CONDITION
1	1	HOLD

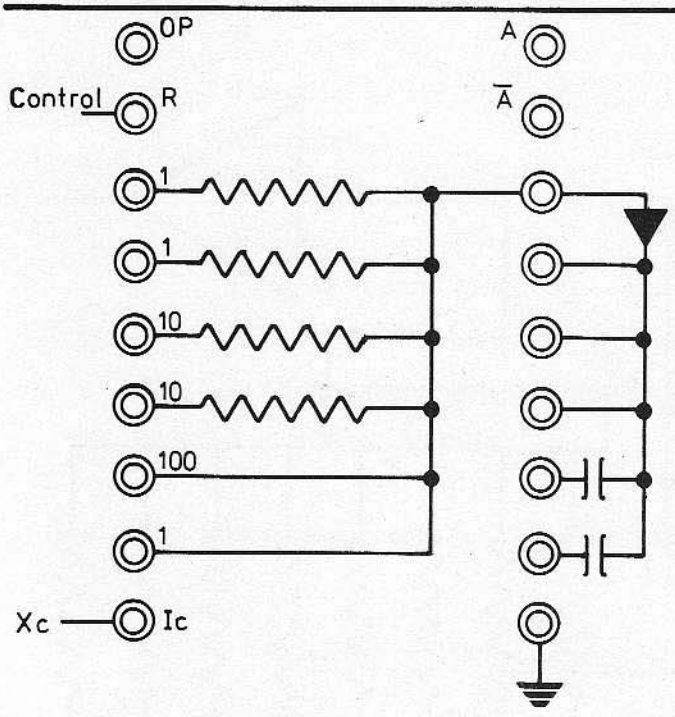
FIG: 9
INTEGRATOR BLOCK DIAGRAM AND FRONT PANEL LAYOUT

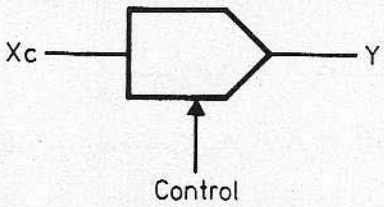




$$Z = -\left[Y + \int_0^t (X_1 + X_2 + 10X_3 + 10X_4)\, dt \right]$$

INTEGRATOR



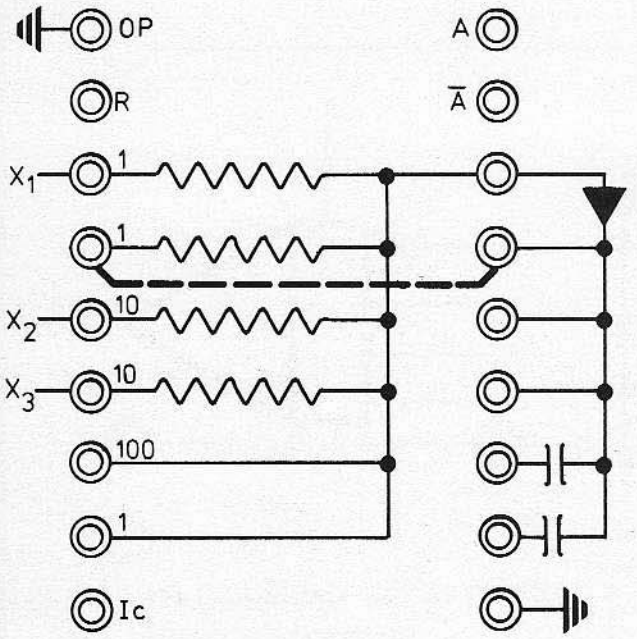


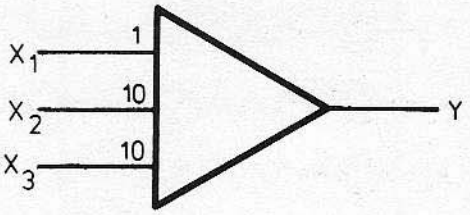
Sample = 0
Hold = 1

SAMPLE & HOLD

INTEGRATOR PATCHING

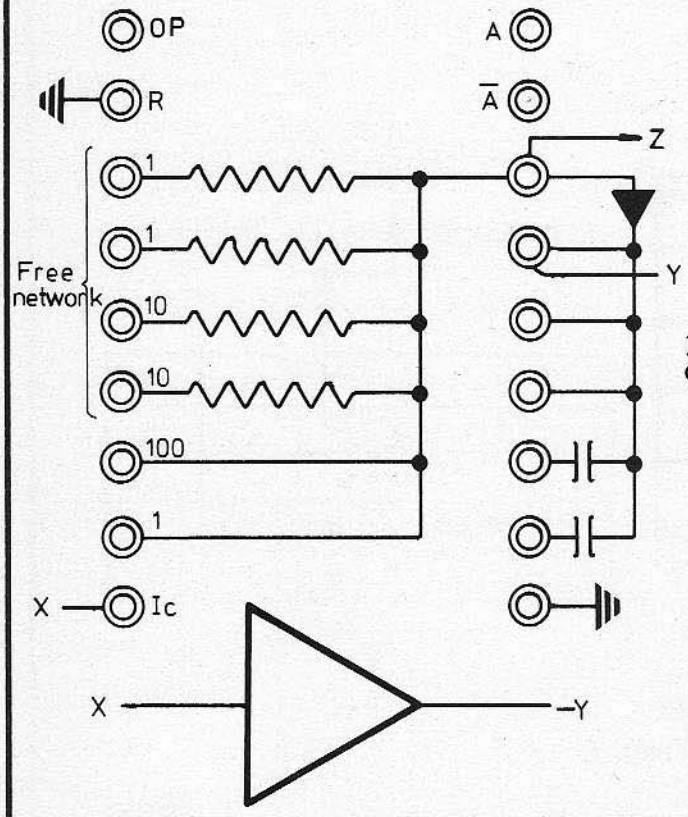
FIG: 10a

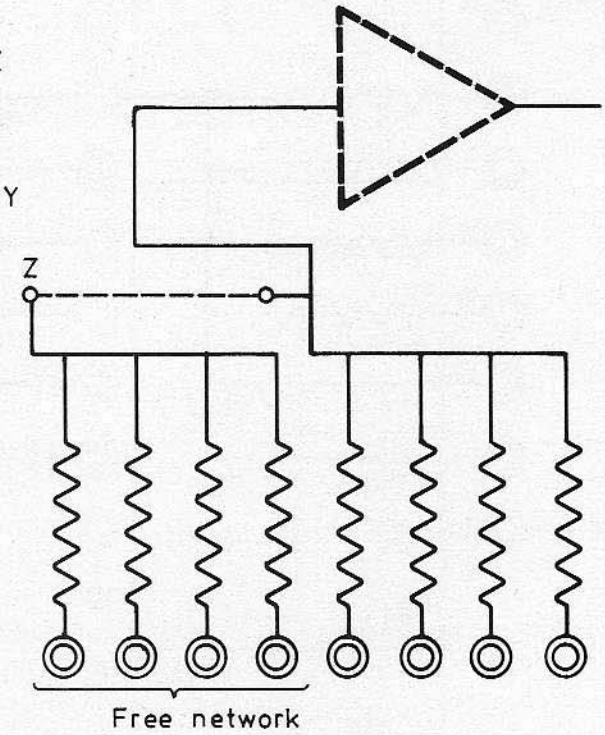




$$Y = -(X_1 + 10X_2 + 10X_3)$$

INTEGRATOR PATCHED AS SUMMER





INTEGRATOR PATCHED AS INVERTER/FREE NETWORK

INTEGRATOR PATCHING

FIG:10b

The computing components may be arranged to give gains of 1 Volt/Sec to 1,000 Volt/Sec. Gain values outside these limits may result in significant degradation of performance.

The integrator may be operated in a number of modes by using the elctronic switches in a different configuration.

The integrator may be operated in the configurations shown in fig's 10a and 10b.

3.2 NON LINEAR PANEL

The Non Linear panel as illustrated in fig. 11 contains the patching outlets for the following components:

a) Reference Supplies
b) Potentiometers
c) Function Relays
d) Comparators
e) Multipliers
f) DFG's
g) Function Board (optional) – Sin/Cos, Log/Antilog, Vector, Free Function

NOTE: These components are not provided with any special monitoring or overload indication features.

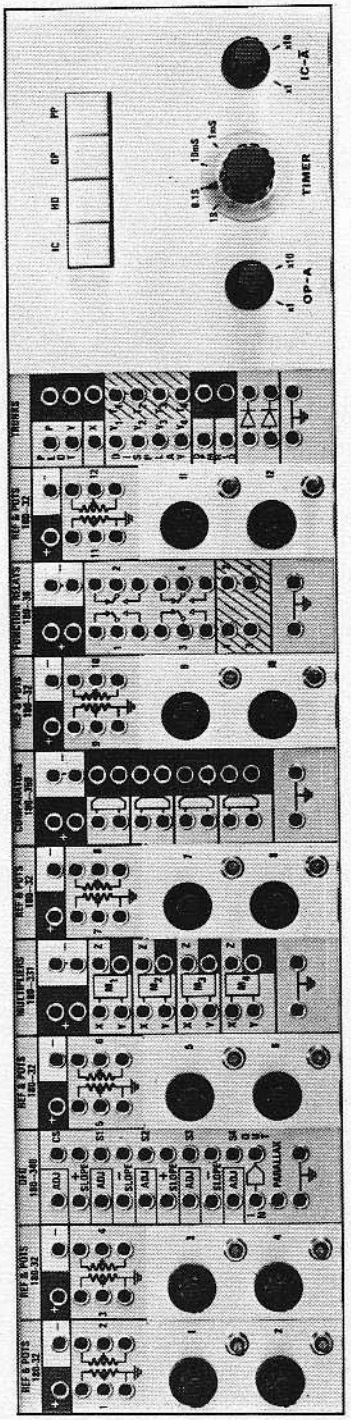
The above components will next be described in detail.

3.2.1 Reference & Potentiometer Panel

Six of these panels are located in the non-linear panel and each contains the following: –

a) +10.00 Volt and –10.00 Volt reference outlets
b) One single ended 10K potentiometer
c) One double ended 10K potentiometer.

The schematic diagram and panel layout is shown in fig. 12.



NON LINEAR PANEL LAYOUT

FIG. 11

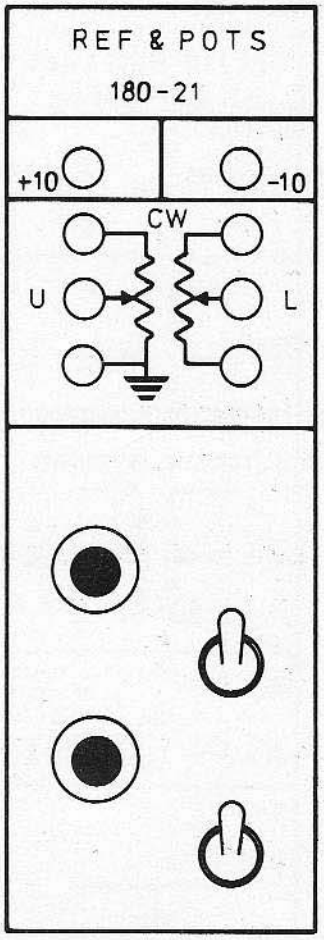


FIG:12
REFERENCE & POT PANEL

3.2.2 Function Relays

This unit contains 4 independent Function relays whose schematic is shown in fig. 13.

These change over switches can be operated by logic signals derived from —

a) Control signals (A) and ($\overline{A}$)
b) Comparator logic outputs
c) Logic signals

3.2.3 Electronic Comparator Panel

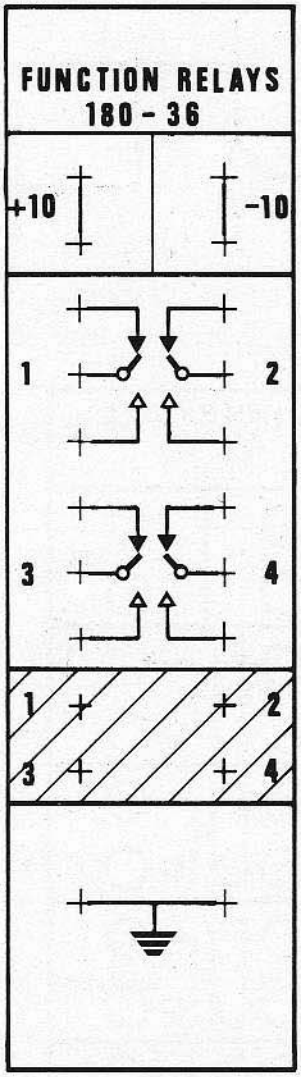
This unit contains four independent electronic comparators whose front panel layouts and schematic is shown in fig. 14.

The function of these units is to provide a means of comparing two analog voltages E_1 & E_2 and produce a logic output which indicates whether

$$E_1 + E_2 < 0$$

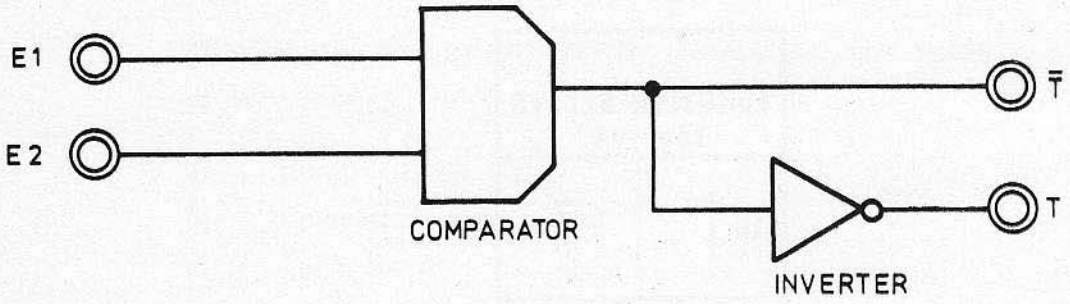
or $$E_1 + E_2 > 0$$

In operation the voltages E_1 and E_2 are applied through '100K input' resistors to the SJ input of a High gain Op amp. If the voltage on the SJ input is positive, then a logic 1 appears on the T output. If this voltage is negative, then a logic 0 appears on T output. This is shown in the truth table on page 40.



FUNCTION RELAYS

FIG:13



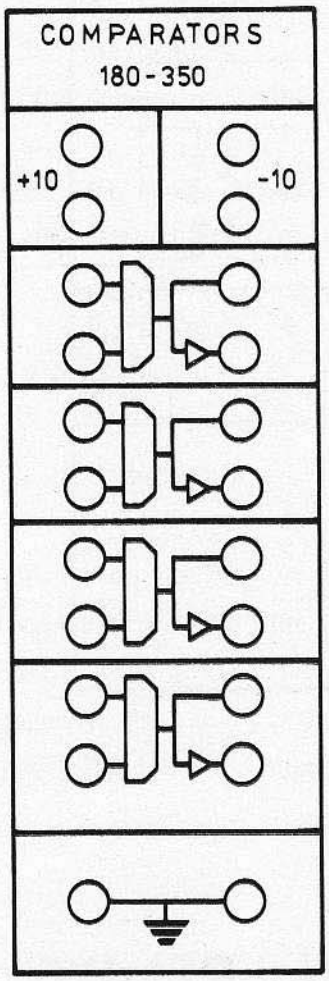


FIG: 14
COMPARATOR FRONT PANEL LAYOUT
AND BLOCK DIAGRAM

Conditions at Inputs	Output	
	T	$\overline{T}$
$E_1 + E_2$ = positive	1	0
$E_1 + E_2$ = negative	0	1

NOTE: Logic 1 = 5V
Logic 0 = 0V

T & $\overline{T}$ are capable of driving 5 DTL loads. The comparator output may be used to control integrator modes or logic circuits.

The outputs of the comparators may be connected ('wired OR') together to produce multiple comparisons.

3.2.4 Multiplier Panel

Each multiplier position can be fitted with either one, two, three or four Multipliers. A block diagram and front panel layout is shown in fig. 15.

The multiplier used is of the transconductance type which produces a product of $\frac{XY}{10}$ in all four quadrants from inputs X and Y.

No external amplifiers are required to perform multiplication, squaring, division or square root operation.

Fig. 16 shows the various multiplier configurations required to perform the different operations.

The multiplier has an accuracy of 1% in all quadrants.

There is one adjustment available on the patch panel see fig. 15, which is —

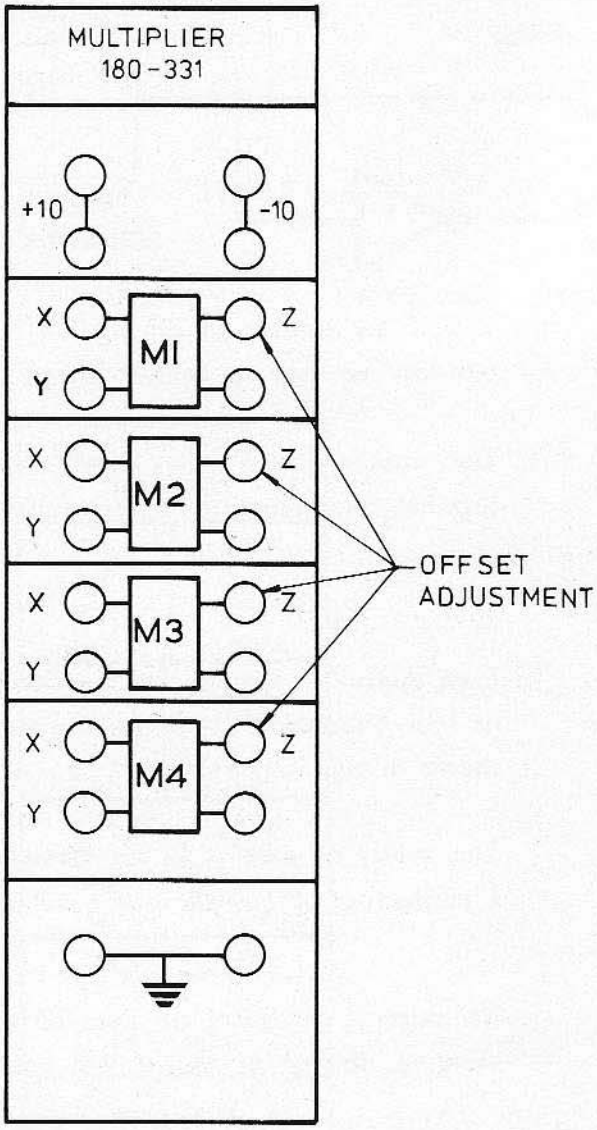
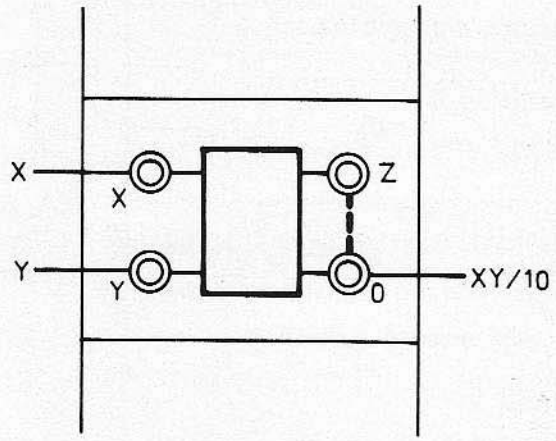
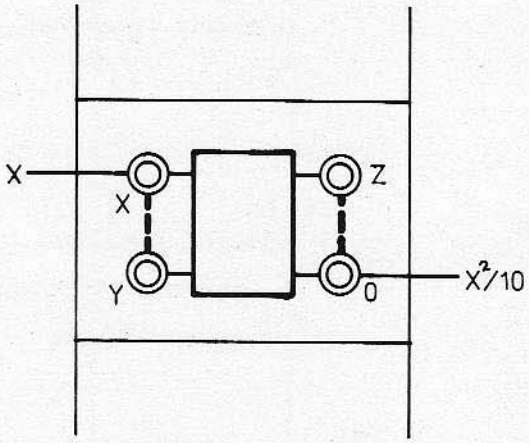


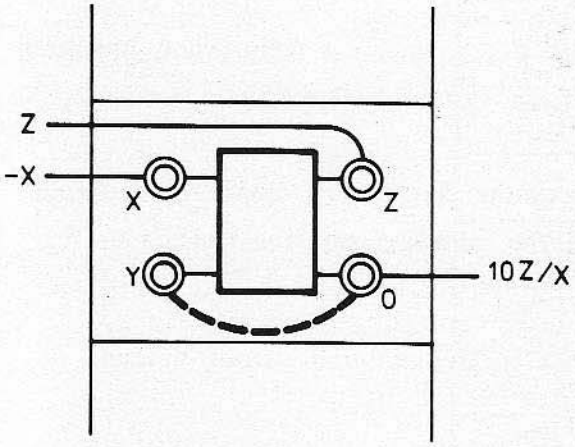
FIG: 15
MULTIPLIER FRONT PANEL LAYOUT



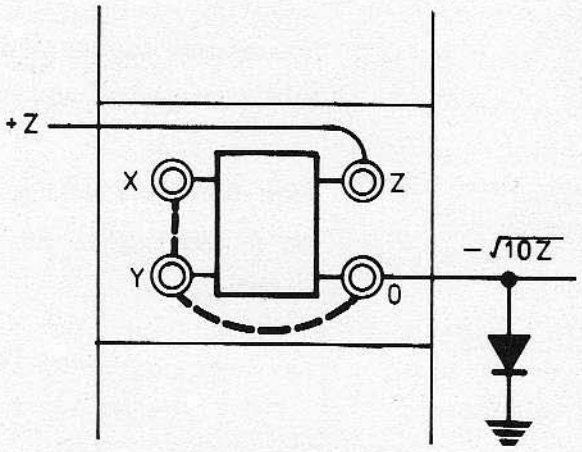
MULTIPLICATION



SQUARING



DIVIDING



SQUARE ROOTING

MULTIPLIER CONFIGUATIONS

FIG:16

Output offset (Null output for zero input)

Internally two other adjustments are available namely –

X Feedthrough
Y Feedthrough

however, these two adjustements have been made in the factory for optimum 4 Quadrant operation and no adjustment should be attempted without reference to maintenance section.

3.2.5 Diode Function Generator

This unit is a fixed breakpoint, variable slope DFG. There are 4 sets of break points located at ± 2 volts, ± 4 volts, ± 6V and ±8V together with a central slope adjustment. The front panel layout and block diagram is shown in fig. 17. Hence if a symmetrical non linearity has to be generated then the unit has effectively 10 segments.

The easiest way to observe this DFG is to use a ramp input, generated by an integrator, which varies from +10 to –10 volts.

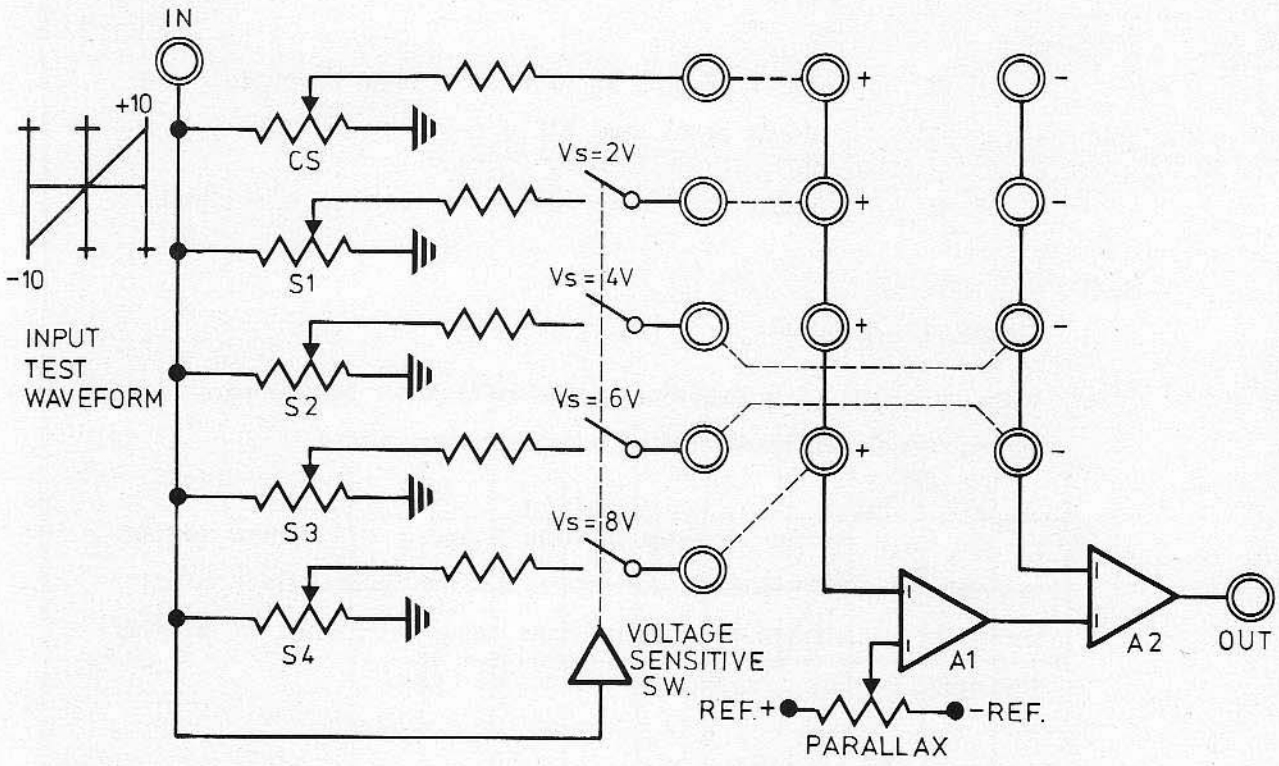
With the above voltage applied to the DFG input, monitor the output on an oscilloscope and perform the following patching and set up operations.

a) Adjust Parallax pot to give required output Y level at Vin = 0.

b) Connect CS to either + slope or – slope to produce + ve. or – ve central initial slope.
Use CS ADJ for desired central slope.

c) Connect S1 to either + or – slope to produce a + ve or – ve slope at 2V point with respect to the central slope.

d) Connect S2 to either + or – slope as above to produce next slope at 4V point.



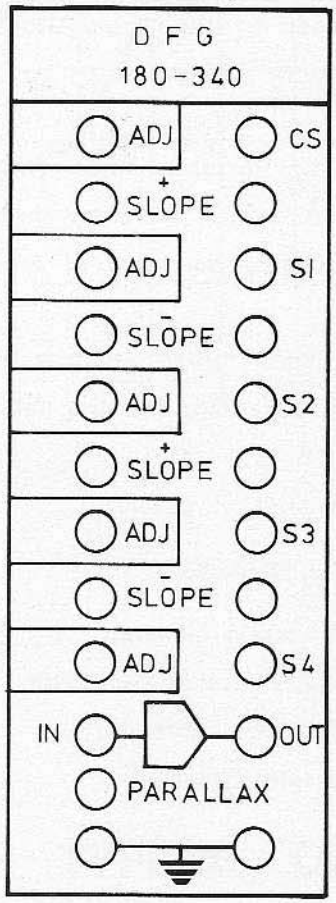


FIG: 17

DFG FRONT PANEL LAYOUT & BLOCK DIAGRAM

e) Connect S3 and S4 to + or − slope to produce last 2 slopes at 6V and 8V.

f) Procedure (c) to (e) should be repeated if required.

Theory of Operation

With zero volts in, the output of the DFG is set by the parallax control which applies an offset voltage on the output.

As the input voltage increases between 0 and ± 2V, a linear output is produced whose slope is determined by the Central slope adjustment, the polarity of the output slope being determined by whether the input current is applied to A1 or A2 input.

When the voltage exceeds ± 2V, the output at the ± 2V breakpoint has slope determined by the S1 adjustment, polarity again determined by the connection to A1 or A2.

As the input voltage increases further, breakpoints at 4V, 6V and 8V operate in succession, each contributing current to A1 or A2 amplifier hence altering the slope of the output voltage at each breakpoint.

A typical output waveshape for the patching of fig. 17, can be observed in fig. 18.

3.2.6 Optional Function Generators

A. Sin/Cos Function Generator
B. Log/Antilog Function Generator
C. Vector Function Generator
D. Free Function Generator

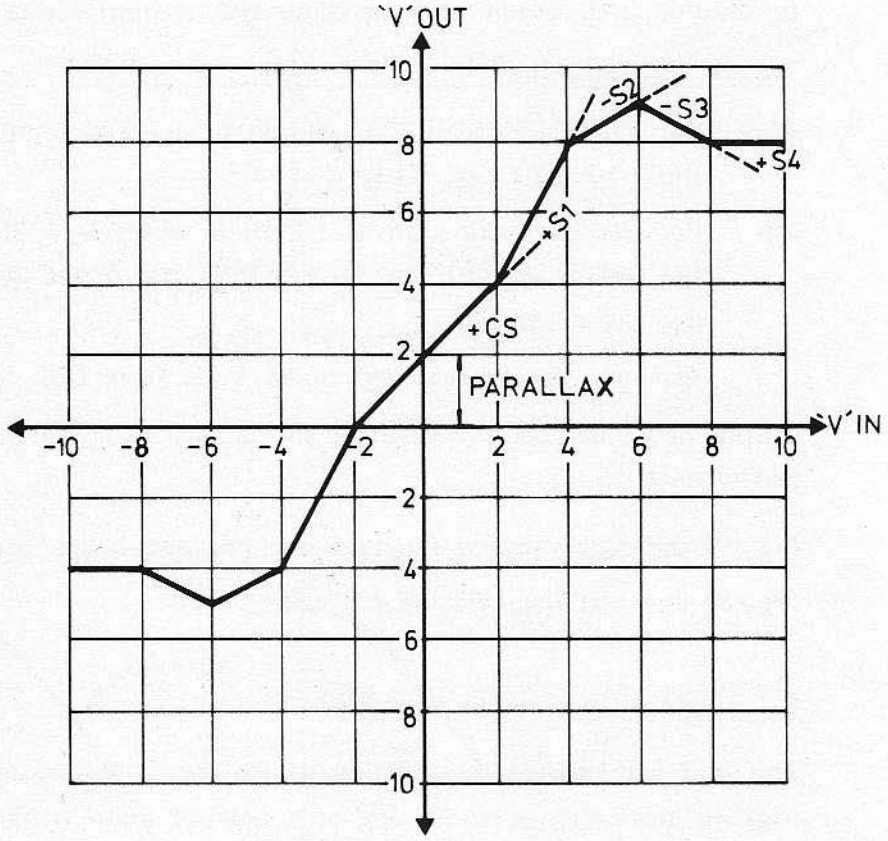


FIG:18 TYPICAL OUTPUT of ±5 SEGMENT DFG

A. Sin/Cos Function Generator

This unit is an analog function module that may be connected to provide various trigonometric gain responses. It provides a D.C. voltage output proportional to the sine of an input voltage where ± 10 Volts of input voltage represents ± 90 degrees of input angle. In addition, the module may be connected to form cosine functions.

Transfer equations are: —

(i) For Sine Function, $E_o = -10 \sin \theta$ where $\theta = 9E_1$ degrees and $-10V \leq E_1 \leq +10V$.

(ii) For Cosine function, $E_o = 10 \cos \theta$ where $\theta = 9E_1$ degrees and $0 \leq E_1 \leq +10$ (for $E_2 = -10V$) and $0 \geq E_1 \geq -10$ (for $E_2 = +10V$).

Accuracy can be expected to be ± 1% from D.C. to 1KHZ.

Output offset has been adjusted at the factory for optimum performance.

Fig. 19 shows the output functions for sine and cosine operation.

Fig. 20 indicates the patching procedure.

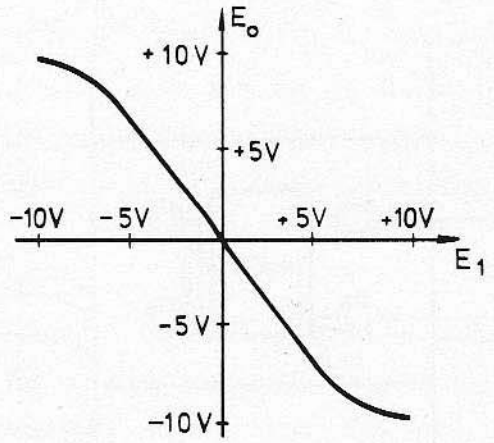
B. Log/Antilog function Generator

This unit will provide computation of the log or antilog of a negative input voltage or the log of a negative input current.

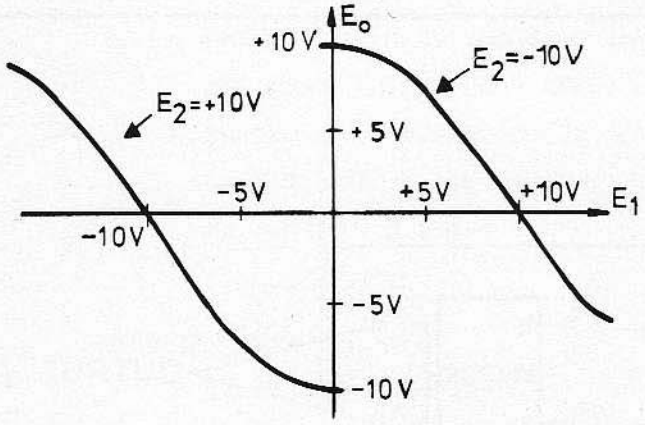
Transfer equations are: —

(i) For Log mode, $E_{out} = -K \log 10 \left(\frac{Ein - Eos}{Eref}\right)$

(ii) For Antilog mode, $E_{out} = Iref.Rf. \ 10^{\frac{-Ein}{K}} \pm Eos.$



SINE FUNCTION



COSINE FUNCTION

FIG. 19

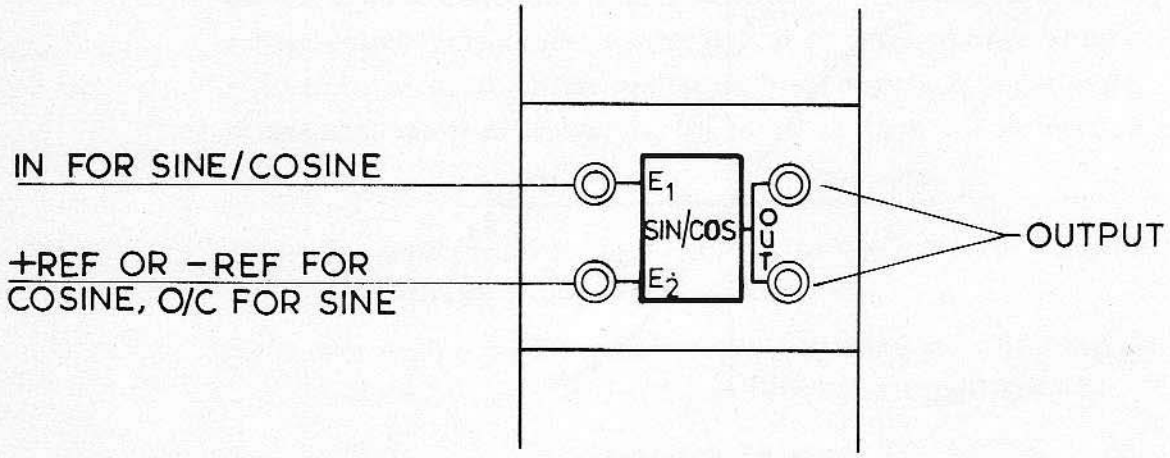
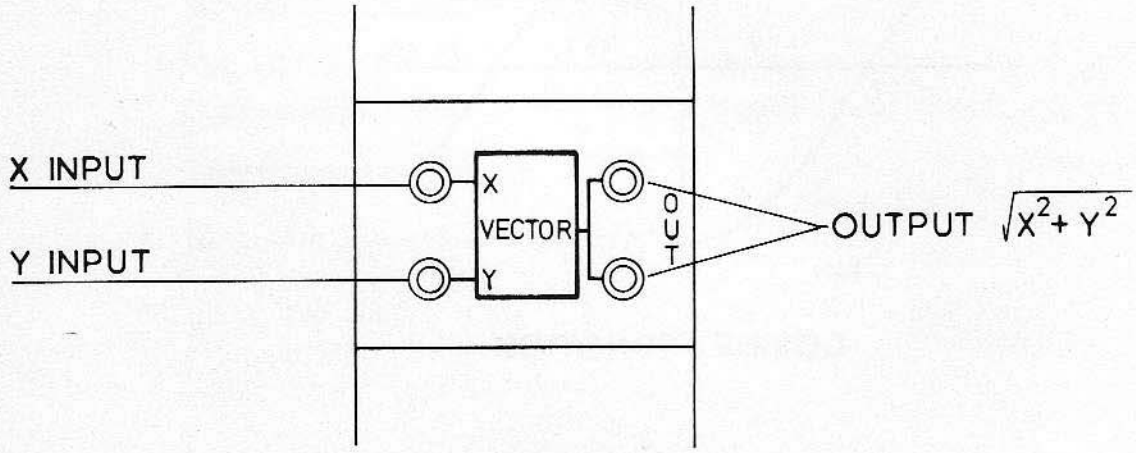


FIG: **20**

PATCHING DIAGRAM FOR SINE/COSINE GENERATOR



PATCHING DIAGRAM FOR VECTOR GENERATOR

FIG: **21**

Input Ranges

Ein = Iin X Rin,

where Iin = −100 pA to −1 mA and Rin = 10K ohms

$-2 < \frac{Ein}{K} < 2.$

E ref @ R in X I ref for Rin = 10K ohms

Decades of input current available, for ± 10V output are defined by ± decades input current = $\frac{10}{K}$.

NOTE:

Amplifier offset (Eos) has been adjusted at the factory. However, for ultimate accuracy, offsets should be checked and adjusted if necessary, so eliminating Eos from the transfer equations.

External Operational Adjustments

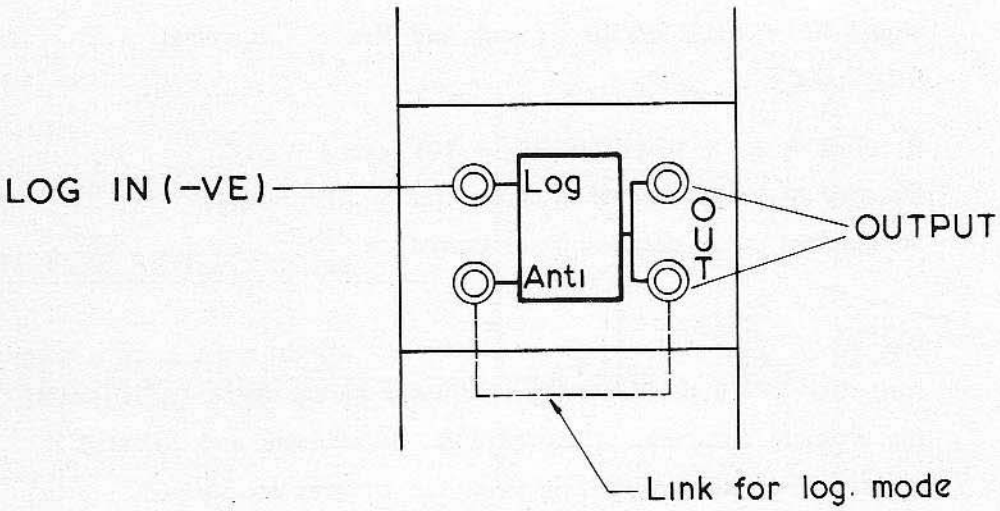
Log Mode

1. Check offset conditions
2. Connect as per Fig. 22
3. Insert an input current equal to the desired reference current, and adjust R2 for Eo = OV.
4. Increase the input current by a factor of 10, and adjust R1 for + k volts at the output
5. Repeat steps 3 and 4

Antilog Mode

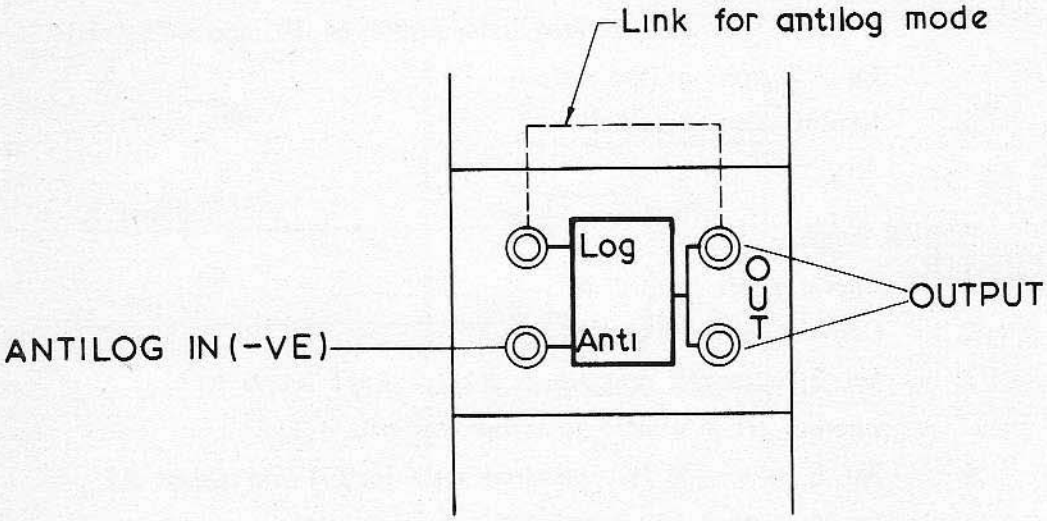
1. Check offset conditions
2. Connect as per Fig. 23
3. Set E in to OV and adjust R2 for Eo=I ref X Rf where I ref = desired reference current.
4. Set E in to −K (K = desired scale factor) and adjust R1 for an output voltage of 10 X I ref X Rf.

Typical 3dB response for I in of 1 uA is 10 KHZ; increasing for higher currents, decreasing for lower currents, down to 8 HZ at 100pA.



PATCHING DIAGRAM FOR LOG GENERATOR

FIG: **22**



PATCHING DIAGRAM FOR ANTILOG GENERATOR

FIG: **23**

Fig. 24 shows the output functions to be expected.

C. Vector Function Generator

This unit is designed to compute $\sqrt{x^2 + y^2}$ based on the instantaneous values of two inputs x and y.
Two units may be connected to compute $\sqrt{x^2 + y^2 + z^2}$

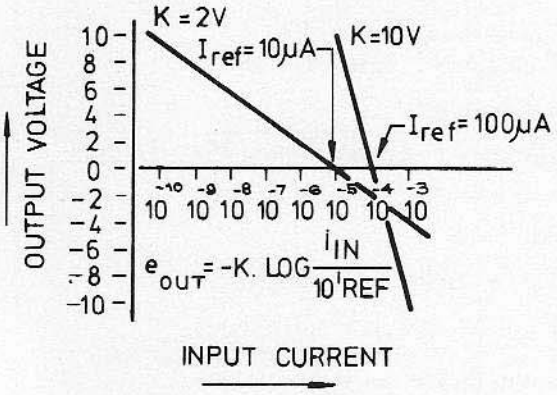
The transfer equation is: —

OUTPUT = K $\sqrt{x^2 + y^2}$ where x = $\pm$ 10V; y = $\pm$ 10V.
OUTPUT = 0 to + 10V.
and K is calibrated internally for scale factor K = 1.
Full scale accuracy is better than 1% with full power response of 10KHZ for 1 degree phase shift.
Output offset has been adjusted at the factory for optimum performance.
Fig. 21 indicates the patching procedure and output functions.

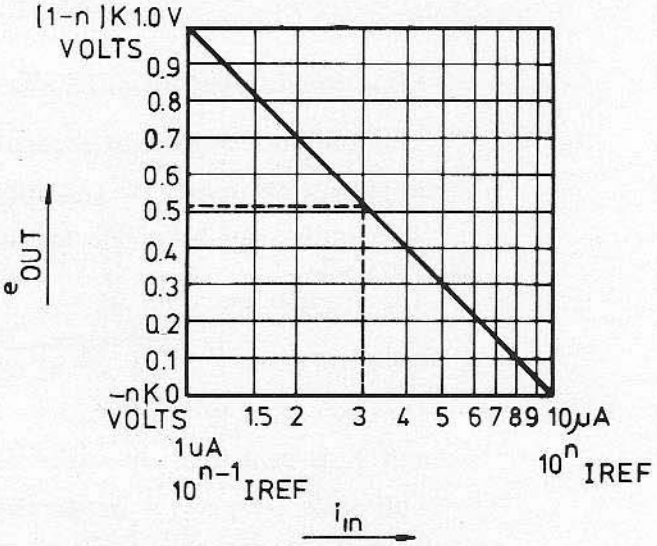
D. Free Function Generator

This consists of an unetched printed circuit board having the facility of supply and input and output terminations.

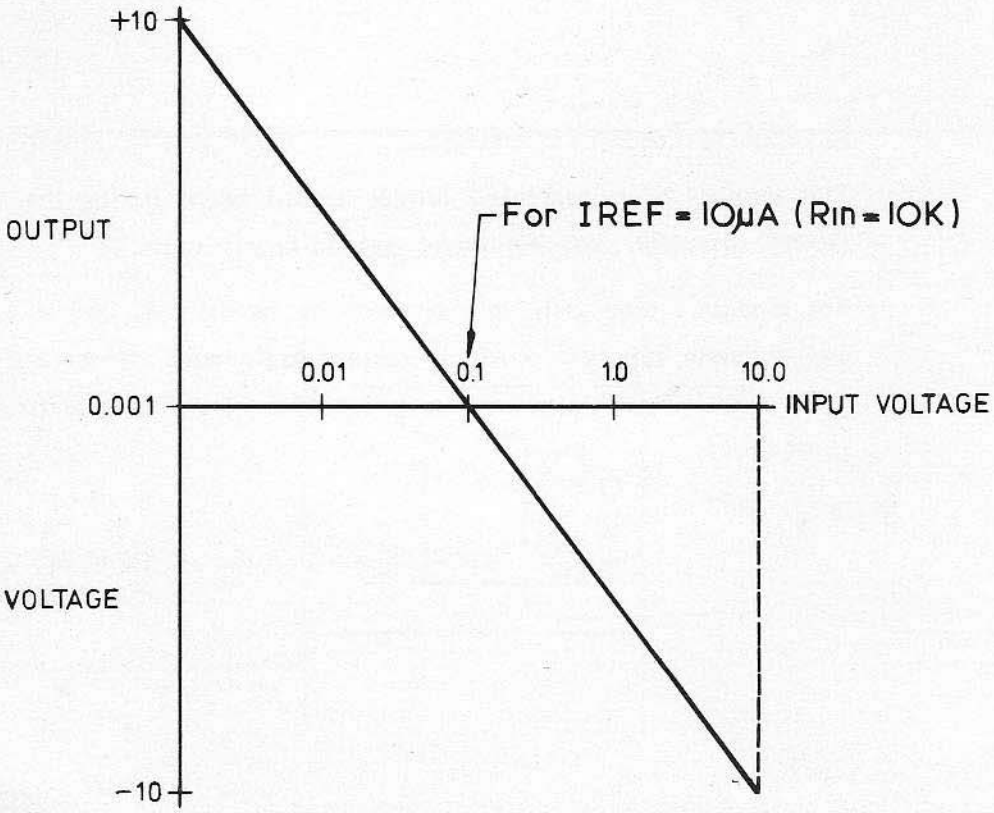
The customer may etch on this card any circuit that uses $\pm$ 15 volt and common supplies, providing current drain does not exceed $\pm$ 20 mA. Input/Output access is available in the relative patch panel area.



LOG OF CURRENT

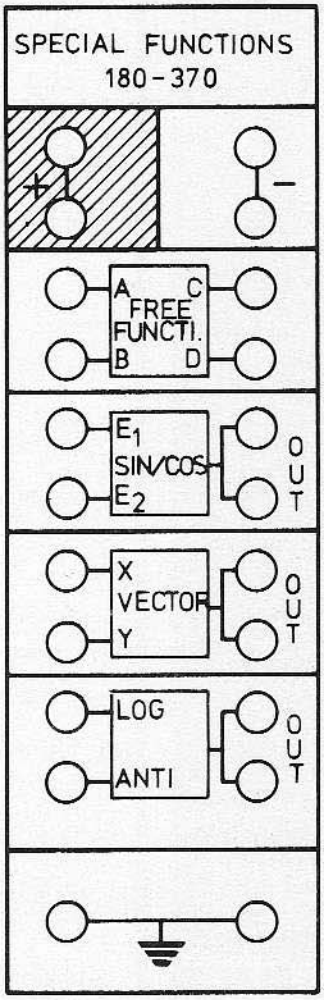


INPUT VS OUTPUT FOR ANY ONE DECADE OF OPERATION



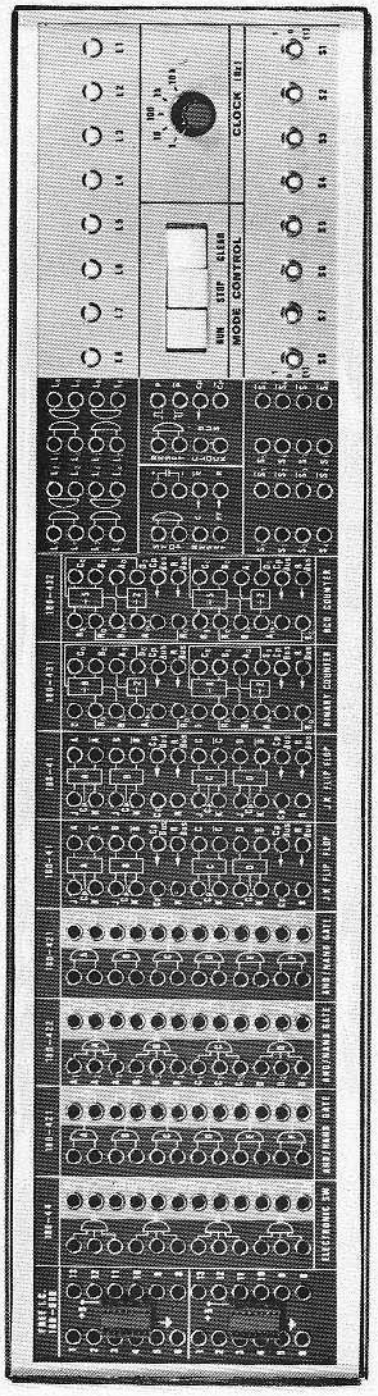
TYPICAL GRAPH OF INPUT VS OUTPUT VOLTAGE
for: IREF = 10μA
ie. EREF = 0.1 Volt
K = 5V

FIG: 24



SPECIAL FUNCTIONS FRONT PANEL

FIG: **25**



DIGITAL PANEL LAYOUT

FIG: 19

3.3 DIGITAL PANEL

The digital panel as illustrated in fig. 19 contains the patching outlets for the following digital components.

3.3.1 J K Flip Flops
3.3.2 Binary Counters
3.3.3 BCD Counters
3.3.4 2 input gates
3.3.5 3 input gates
3.3.6 Electronic switches
3.3.7 Free Integrated Circuit position

A description of the above components follows.

3.3.1 Quad J K Flip Flops

This unit contains 4 TTL, J K Master/Slave flip flops which are arranged as shown in fig. 20.

The Master section accepts information from J and K when clock pulse goes high and uses this information, together with feedback from Q and $\overline{Q}$, to set the Master Latch.

When the clock pulse falls to a logical "0", this information is transferred to the slave latch and to the outputs.

The J K flip flop truth table is shown below.

J	K	Qt + 1
0	0	Qt
0	1	0
1	0	1
1	1	$\overline{Q}$t

QT = Flip Flop state before arrival of clock impulse

Qt+1 = Flip Flop after arrival of clock pulse

The Flip Flops used are identical to type SN 7473, and manufacturers data sheets on this type of J K Flip Flop will give more detailed information.

NOTE: Outputs cannot be wired for 'OR' Operation

These Flip Flops can be connected to form

a) Binary counters
b) Shift Registers
c) Storage Registers
d) B C D counters

3.3.2 Hex 2 Input Gates

This section consists of 6 independent 2 input AND gates with inverted outputs, the block diagram and patching layout is shown in fig. 21.

Each gate output can drive 8 'unit' logic inputs and can be wired OR'd as shown in fig. 21.

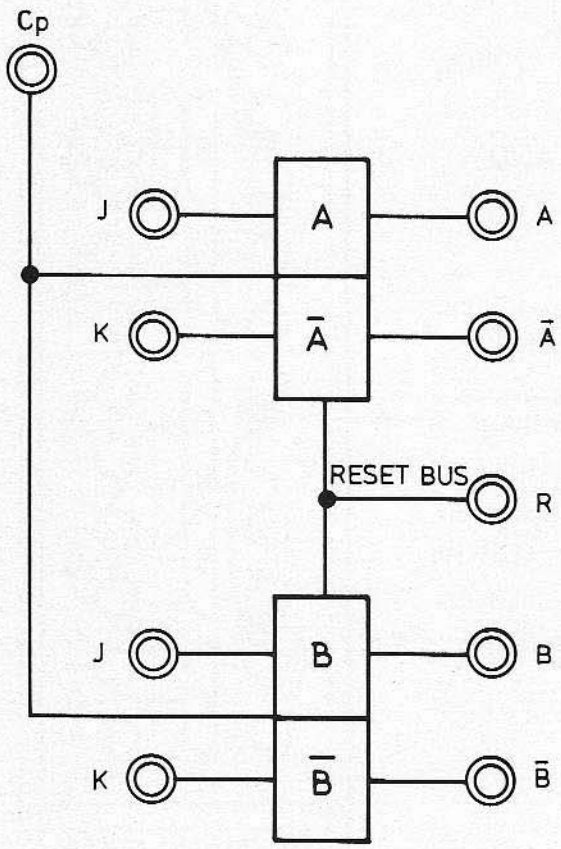
3.3.3 Quad 3 Input Gates

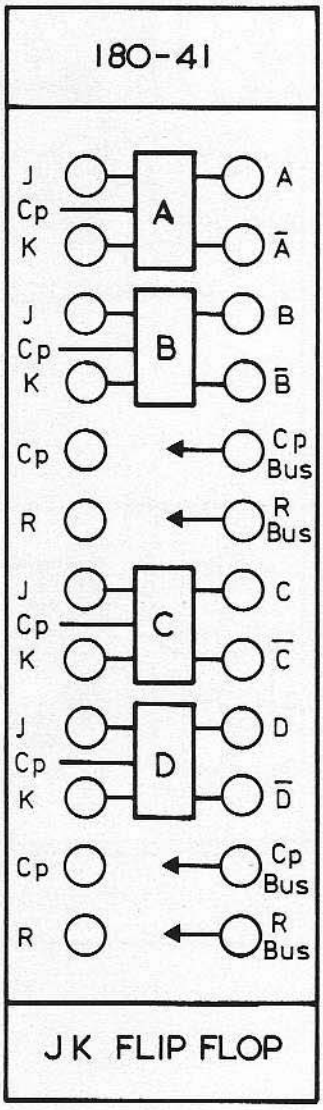
This section consists of 4 independent 3 input NAND gates, two of which are provided with inverters, as shown in fig. 22, to give an AND function.

Outputs can be wired OR'd and can drive up to 8 logic inputs.

3.3.4 Dual 4 Stage Binary Counter

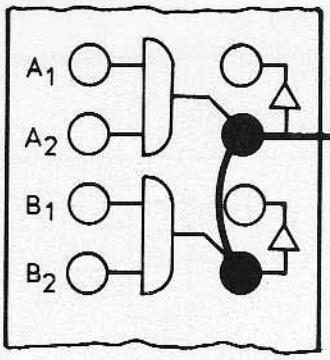
This section consists of 2 independent 4 stage binary counters which are divided into 2 stages as shown in fig. 23.



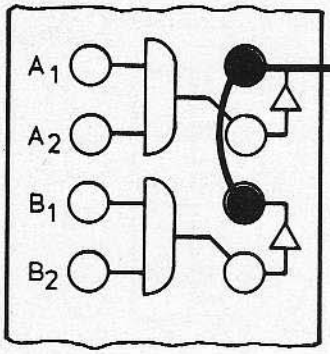


FLIP-FLOP BLOCK DIAGRAM AND PATCHING LAYOUT

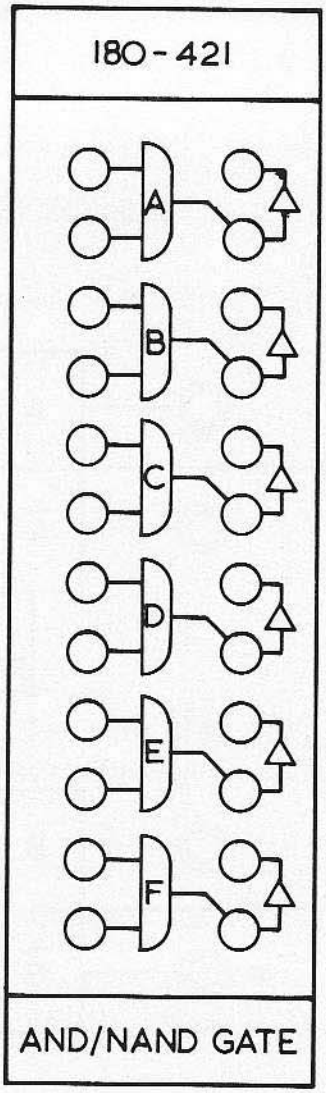
FIG: 20



WIRED AND



WIRED OR'D

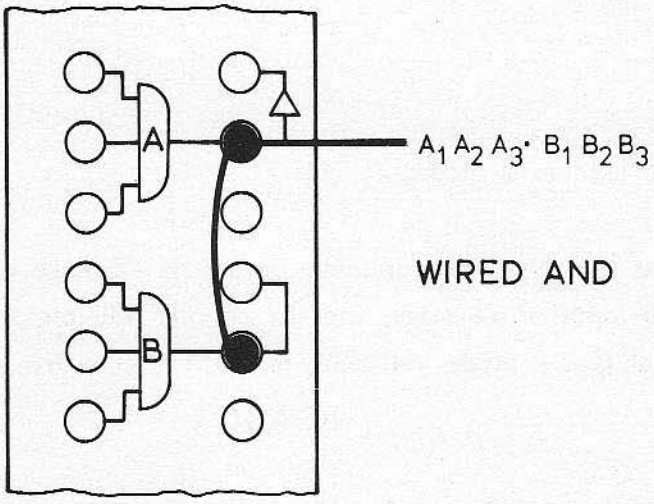


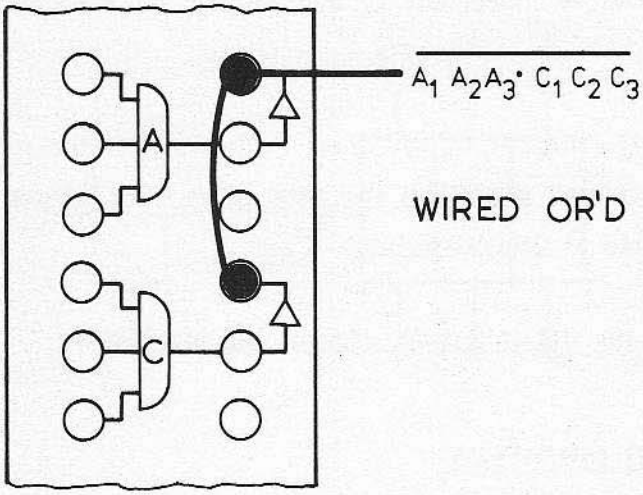
A_1	A_2	A_o	$\overline{A_o}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

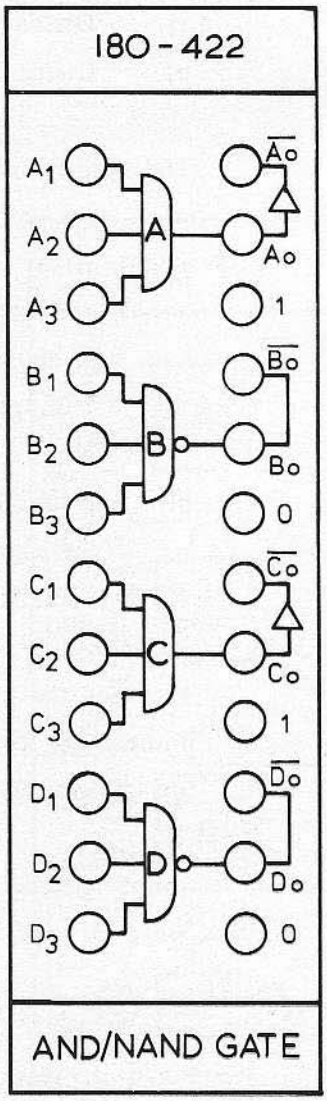
TRUTH TABLE

2 INPUT GATE PATCHING LAYOUT AND TRUTH TABLE

FIG:21







A_1	A_2	A_3	A_o	$\overline{A_o}$
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

TRUTH TABLE

3 INPUT GATE PATCHING LAYOUT AND TRUTH TABLE

FIG: 22

a) Divide by 2
b) Divide by 8

The counter can be used in 2 modes.

a) When used as a 4 bit binary counter, output of ÷2 stage is connected to input of ÷8 stage, and the counter will perform in the normal binary mode, returning to 0000 after every 16th pulse.

b) When the above connection is not made, the two sections of the counter can be independently used for ÷2 and ÷8 binary operation.

To reset the counter, a logic 1 or 0/C must be present on the reset input. For proper counter operation, the reset input must have a S/C to ground or logic 0 connected to it.

Counting occurs on the negative going edge of the input pulse.

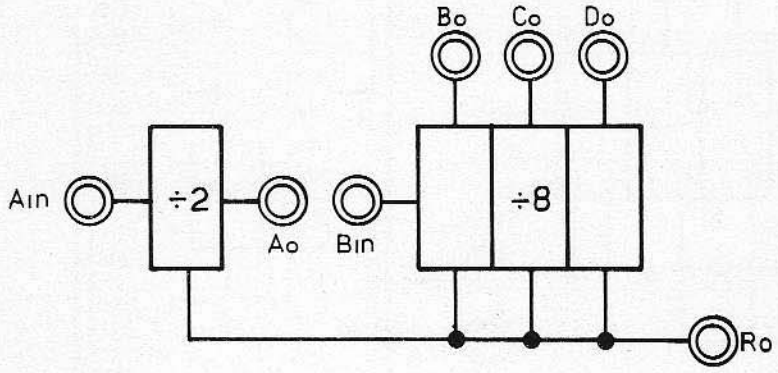
3.3.5.0 DUAL BCD COUNTERS

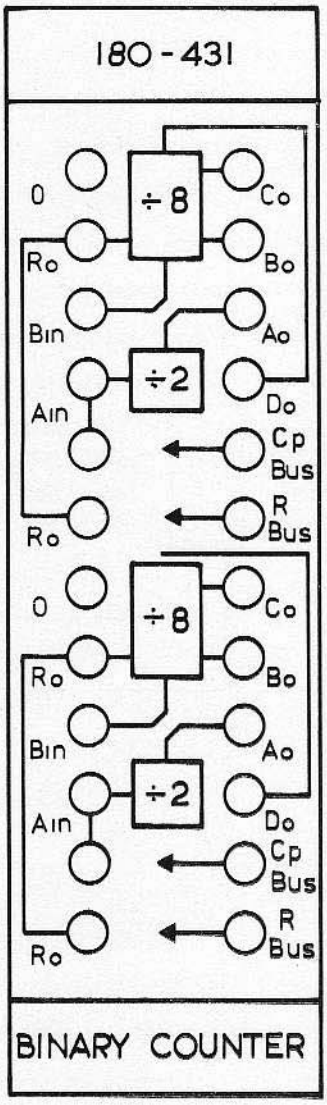
This section consists of 2 BCD counters which are divided into 2 stages as shown in fig. 24.

a) Divide by 2
b) Divide by 5

The counter can be used in 3 modes.

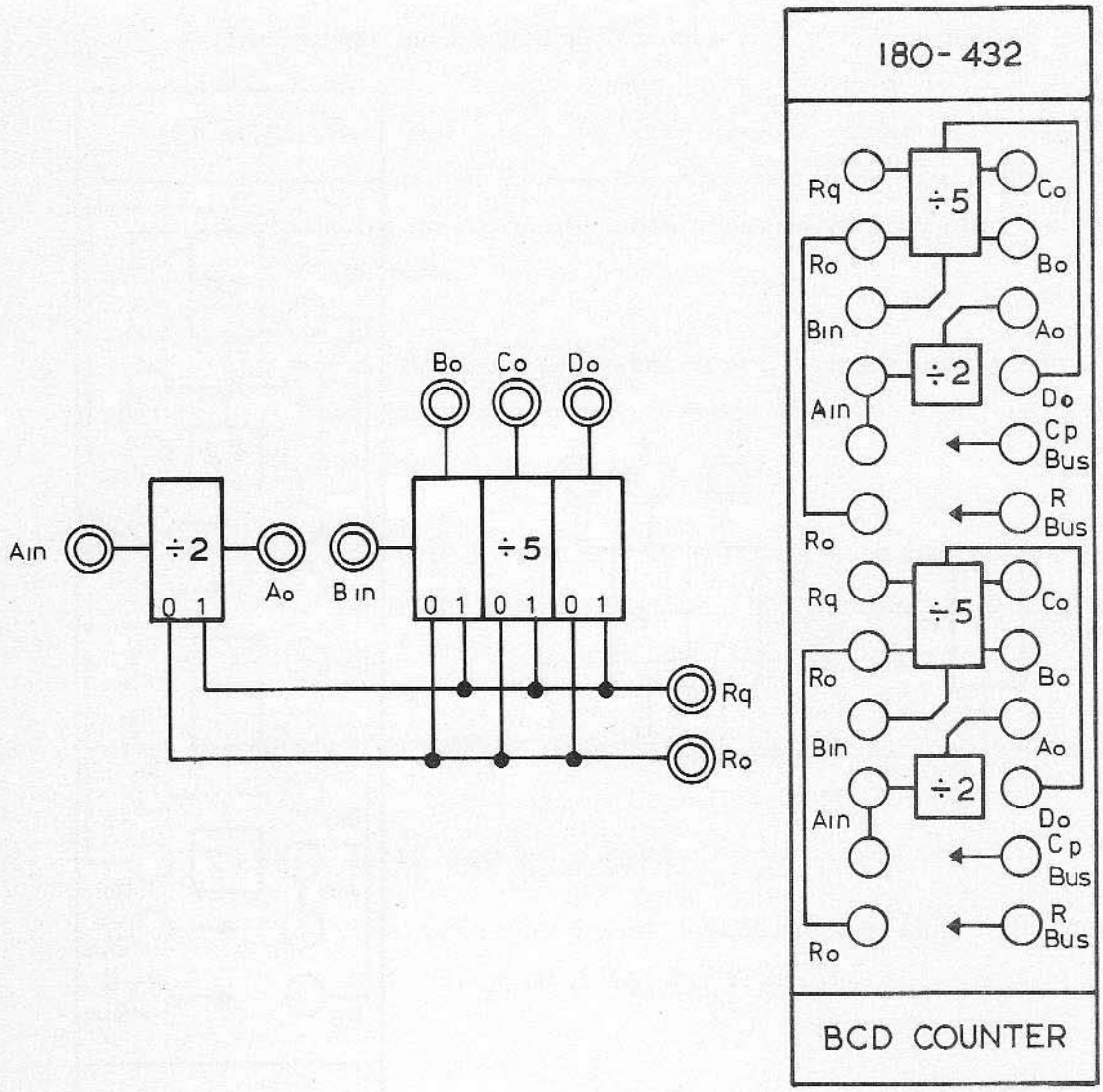
a) BCD decade counter, by connecting output ÷2 stage to input of ÷5 stage. Under this condition the counter will operate as an 8421 BCD counter.





BINARY COUNTER BLOCK DIAGRAM AND PATCHING AREA

FIG:23



BCD COUNTER BLOCK DIAGRAM AND PATCHING AREA

FIG:24

b) Symmetrical Divide by 10 operation. Connect the output of the last stage (D) to the input of 1st stage (A). When pulses are applied to the ÷5 stage, a symmetrical waveform, one tenth of the applied frequency, will appear at the 'A' stage output.

c) If no external connections are made the counter can be used as a divide by 5 and divide by 2. This counter can be reset to either BCD "O" or BCD "9" by having either a logic 1 or an O/C on the corresponding input. For proper counter operation both Reset inputs should have a logic 0 or S/C to ground connected to them.

Counting occurs on the negative going edge of the input pulse.

3.3.6.0 QUAD ELECTRONIC SWITCH

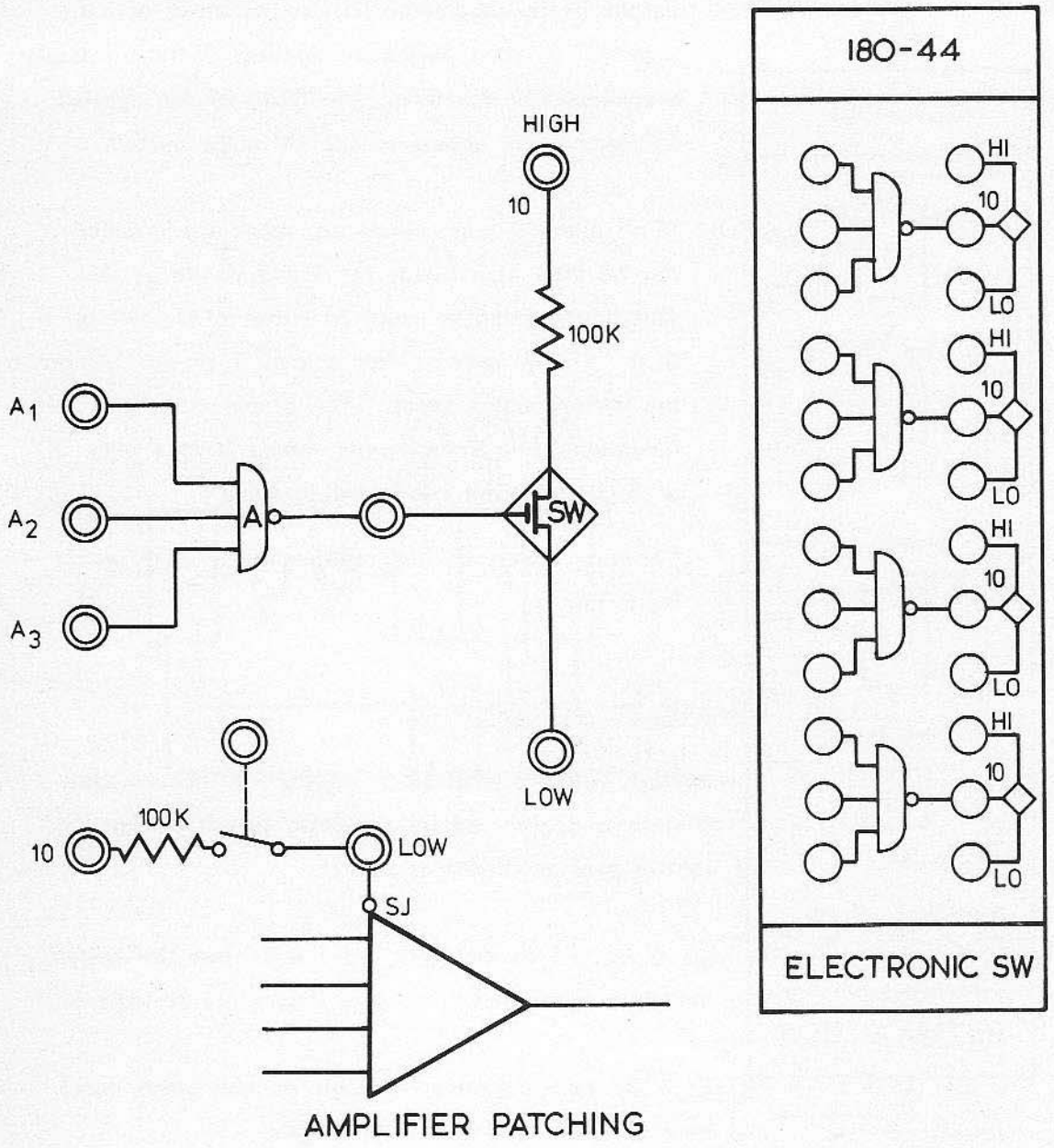
This section contains 4 gated 3 input electronic switches whose state is determined by the logic signals present on the control gate as shown in fig. 25.

A logic 0 applied to any gate input will open the switch. The switch is closed when all gate inputs are at logic 1.

NOTE: The gate output is available on the patch panel and may be used as a logic NAND gate.

In operating the electronic switch, the low terminal must be connected to an amplifier summing junction and the signal is applied to the high terminal.

NOTE: A 100K input resistor is connected in series with the switch.



AMPLIFIER PATCHING

ELECTRONIC SWITCH BLOCK DIAGRAM AND PATCHING AREA

FIG:25

CHAPTER 4

MAINTENANCE

4.1 MAIN FRAME

This section provides maintenance information for the power and reference supplies.

These provide the following outputs:

± 15 V.D.C.	—	Regulated Analog I.C. Supply
± 10 V.D.C.	—	Regulated Reference Supply
+ 5 V.D.C.	—	Regulated Digital I.C. Supply

CIRCUIT DESCRIPTION

Primary power is connected to the EAI 180 by a three wire cable. One side of the AC line is routed through the POWER switch on the REAR panel, to the primary of Transformer T1. The primary windings can be connected for 230V or 115V operation.

The Digital Panel Meter is supplied from the auxiliary supply mounted on the right hand rear of the cabinet. This supply consists of a transformer T1, Rectifier MR3 and smoothing capacitors C13 & C14. This is then regulated by IC6, a 5volt Regulator. (This supply will be incorporated in the main power supply for units of serial nos. higher than 280).

As the main regulator circuits are similar in the ± 15V and a ± 10V supplies. the following description will be confined to the + 15V and + 10V section.

An unregulated D.C. supply is provided by Bridge rectifier MR1 and capacitors C1 and C2. This source is then passed through the series regulator IC1 to provide the +15 regulated output. A level stabilising capacitor C6 is across the output.

The + 10V regulator consists of IC4 as a shunt regulator driving into Q6 and providing output. Output level adjustment occuring through VR2, varying the feedback ratio for IC4, initial reference being picked up from IC3. The + 10V reference is then applied to IC5 driving into Q7.

Adjustment occurs by varying the input/Feedback ratio of IC5 by means of VR3.

The + 5V logic supply is provided by IC3 providing regulation to Q3 and hence Q4 to output via current limit resistor R3.
Output adjustment occurs via VR1.
A level stabilizing capacitor C9 is across the output.

EXTERNAL ADJUSTING is only available on the ± 10 reference supply at VR2 and VR3, accessible through the rear panel.

SLAVING FACILITY — T3

The slaving connector is situated at the right hand side/rear of the cabinet.

Available terminations are:

(i) A H.Q. ground line,
(ii) A hold line,
(iii) Operate/Reset lines.

When either the free plug or the red plug of the slave cable are inserted in the cabinet socket of the master computer, the operate/reset lines will be available to the amplifier panel. The slave computer, however, will utilize the operate/reset, hold and H.Q. ground lines of the master computer, thus causing the slave unit to be fully controlled from the master.

Trunking & Display Facility

The TRUNKS connector, T2, is situated on the right hand rear of the cabinet and has terminations suitable for driving an X-Y plotter.

Available terminations are:

(I) 4 free trunk lines T1, T2, T3, T4;
(II) X line for X axis;
(III) Y line for Y axis;
(IV) P line for pen control (i.e. pen lift on I.C.);
(V) H.Q. ground line.

The DISPLAY connector, T1, is situated on the right hand rear of the cabinet and has terminations suitable for driving the EAI slow scan oscilloscope.

Available terminations are:

(I) X line for the X axis;
(II) 4 Y lines for the Y axis of each channel;
(III) H.Q. ground line;

All slaving, trunks and display lines are to be connected via the trunks area on the non-linear panel.

4.2 LINEAR PANEL

METERING & SWITCHING CIRCUITS DESCRIPTION

A digital panel meter using a 7 segment readout is used for all measuring at an accuracy of 0.05% $\pm$ 1 digit.

These switch positions give the following conditions for SW1,

Pos. 1 — P B; this allows any single ended pot settings to be observed on the meter provided the Pot Bus switches are depressed.

Pos. 2 — VM; this allows external signals to be measured on the Meter using the VM input socket in the trunks area.

Pos. 3 — AMP; this allows the amplifier output to be measured on the meter.

Pos. 4 — BAL; this allows the balance relays to operate enabling amplifier balancing.

SW3 — Positions 1 to 12 — Amplifier Outputs switched to the DPM and the Trunk panel socket.

Pos's 1 to 12 — Amplifier Outputs switched to the DPM and the Trunk panel socket.

OVERLOAD DETECTION CIRCUIT

The detection circuit consists of a dual comparator integrated circuit driving a transistor switching the overload indicator lamp to ground.

The switching is effected by a positive output from the comparator, this level only occurs when the input at the comparator pin is greater than $\pm$ 2V. This causes the output level change due to the differential inputs of the comparator being biased at + and — 2V. These $\pm$ 2V levels are picked up from a divider network across the $\pm$ 15V supply and the lamp switch-on levels can be adjusted at these networks by means of VR1 and VR2.

The overload/hold circuit is effected by the ground level at the switched transistor being found on the external overload socket found on the trunks panel. This is patched, if required, into the hold socket, thereby grounding the mode control gates and causing a hold condition.

INTEGRATOR CIRCUIT DESCRIPTION

The operate transistor Q4 and the reset transistor Q1 control the mode of operation of the integrator. The transistors are energised by the A & $\overline{A}$ signals which are controlled by the mode control pushbuttons on the control panel.

When the mode control switch is set to the RESET position, transistor Q4 is turned off and the inputs to the integrators are O/C. None of these inputs can affect the amplifier. Transistor Q1 is energised and it connects the junction point of R1 and R15 to the summing junction of the amplifier. The feedback network for the amplifier consists of R15; R1 is the input resistor. A voltage E_{ic} applied to the IC termination establishes a voltage E_o at the output of the amplifier. In the steady state, the amplifier behaves as an inverter and has an output of $-E_{ic}$. With + 5 volts patched into the IC terminal the steady-state amplifier output is — 5 volts. If no voltage is applied to the IC terminal, the amplifier output is zero.

In the HOLD mode, both Q1 and Q4 are O/C. The summing junction of the input resistors is O/C and the initial condition input is removed. If an initial condition voltage has been applied (in the RESET mode) this voltage will remain. Alternatively, the integrating capacitor remains charged to the voltage attained in the OPERATE mode.

In the OPERATE mode, transistor Q4 is S/C and connects the summing junction of the input resistors to the SJ of the amplifier. The integrator is operational. To summarise, an initial condition voltage is applied to the integrator in the RESET mode. The output voltage is equal in magnitude and opposite in polarity to the IC input. In the HOLD mode, all inputs to the integrator are removed and the output remains as the voltage applied as an initial condition, or holds the voltage reached during the OPERATE mode. In the OPERATE mode, the inputs are applied, and integration with respect to time takes place.

Amplifier offset is adjusted by RV1, feeding a negative level into the offset terminals of the amplifier.

Balance relay K1, connects R20 as feedback and R16 to ground for balancing conditions.

DUAL SUMMER CIRCUIT DESCRIPTION

The dual summer is two identical circuits each consisting of an operational amplifier, an input/Feedback resistor network (R1 — R5) and an offset adjusting circuit.

The offset adjustment circuit consists of VR1 applying an adjustable negative level to the amplifier offset terminals.

Balance Relay RLA1, connects R8 as feedback and R6 to ground for balancing conditions.

Amplifier gain is selectable from 0.1 to 10 and always inverted.

4.3 NON-LINEAR PANEL

MODE CONTROL CIRCUIT DESCRIPTION

The basic theory of the mode control circuit is to use pushbutton switches to apply levels to a 4 input gate, the gate outputs being used to drive the integrator switches.

Manual control is effected as follows:

Reset condition is effected by switching SW2/2, grounding Pin 2 of IC4 and producing a '1' output at Pin 6. This output level is fed back to Pin 9 of IC4, producing an '0' output at Pin 8 as all other gate inputs are O/C.

HOLD condition is effected by switching SW2/3, grounding Pin 2 of IC5 causing a '1' output on Pin 6 of IC5 and Pin 10 of IC5, hence a '0' output at Pin 8 of IC5. This level is transferred to Pins 5 and 10 of IC4, causing '1' conditions on Pins 6 and 8 of IC4 thereby effecting the hold mode.

OPERATE condition is effected by switching SW2/1, grounding Pin 12 of IC4 and producing a '1' output at Pin 8. This output level is fed back to Pin 4 of IC4, producing an '0' output at Pin 6 as all other gate inputs are O/C.

REPETITIVE OPERATION condition is effected by switching SW2/4. This applies a ground to Pin 9 of IC5, thus indicating the rep-op condition via L3, and switches the rep-op generator output into the detector circuit of IC2 and IC3.

This rep-op output integrates until a + 10 volt level is reached. This point is detected by IC3, due to a differential input of — 10V, and a level change from a '1' to an '0' occurs. This '0' level causes the RESET mode to occur, resetting the rep-op generator to zero. When the rep-op generator output reaches zero, IC2 detects this level due to a differential input of zero, and a level change from a '1' to an '0' occurs. This '0' level causes the operate mode to occur, resetting the rep-op generator to the operate condition.

The RESET, HOLD and OPER lamps in the P.B. switches are turned on by the output states of gates IC4 and IC5.

REPETITIVE OPERATION GENERATOR CIRCUIT DESCRIPTION

The rep-op generator is effectively an integrator, suitably modified by having a selectable combination of resistors and integrating capacitors. Variable voltages to operate and reset inputs, supply the between range adjustments. The operate and reset control levels are connected permanently from the mode control signals A & $\overline{A}$. The output of this generator can be monitored at the ramp output socket on the Trunks panel.

POT GROUPS

Each pot group consists of one single ended pot and one double ended pot. Each pot has one momentary action change-over switch for POT BUS monitoring of settings. These switches, when actuated, place + 10 volts at the top of each pot and place the outputs onto the POT BUS line.

FUNCTION RELAYS

Operation is effected by placing a '0' on the control line, resulting in a '1' level at the inverter output and a '0' level at the gate output, so causing relay actuation and a change over' condition to occur.

QUAD COMPARATOR CIRCUIT DESCRIPTION

This circuit consists of a precision comparator integrated circuit IC1. One input of the comparator is taken to ground via a resistor, and the other to two 100K precision resistors to which the inputs for comparison are connected.

Operation is effected when the sum of the inputs equals zero and a change of output state is observed. If input sum is +ve a '1' output will occur; if input sum is –ve a '0' output will occur. Output inversion occurs through the Q1 & Q2 configuration.

MULTIPLIER CIRCUIT DESCRIPTION

The multiplier circuit consists of an encapsulated 426A analog multiplier/ divider of 0.6% maximum overall accuracy, an offset and two feedthrough adjustments.

Balancing of the X & Y feedthroughs has been fixed at the factory thus leaving one control, for offset only.

BALANCING PROCEDURE

Set X = 0, Y = 0, and adjust output offset to zero volts DC output. No other adjustments are necessary.

This multiplier (426A) has non-linearity and feedthrough of 0.3% each for maximum Y, and drift of $\pm$ 2mV/^{o}C.

If inputs, greater than $\pm$ 10.5 volts are to be used into the multiplier, they can be attenuated by a resistor in series with an input terminal. This changes the scale factor of the multiplier, e.g., if a 10K resistor is used in series with one of the inputs the scale factor would be halved giving the transfer equation : Output = $\frac{XY}{20}$. Note: maximum input voltage = $\pm$ 18V.

DFG CIRCUIT DESCRIPTION

This is a fixed breakpoint, variable slope type DFG. The breakpoints are fixed at $\pm$ 2V, $\pm$ 4V, $\pm$ 6V and $\pm$ 8V with a central slope adjustment to set the initial slope at point Y = 0.

Input is driven through IC1 at a gain of −1, then through the transistor combination Q1, Q2 to give current drive to the zeners and diodes providing the voltage breakpoints. A combination of forward and reverse voltage drops in the diode networks provide the breakpoint voltages.

As a breakpoint is reached, the voltage output adjusts via the appropriate VR. Breakpoint polarity is selected by patching the breakpoint output into either IC2 or IC3.

Parallax control VR6 selects the central slope voltage level, variable from +10 to −10.

SPECIAL FUNCTIONS CIRCUIT DESCRIPTIONS

A. Sin/Cos Generator

This circuit consists of a 'Black Box' module, used in conjunction with a precision input resistor network and an offset adjusting potentiometer.

The module is a two quadrant arc-sine transconductor, output current being a straight line approximation to an arc-sine function. The resistor is used on the E2 input to provide shift for cosine functions. The potentiometer is used for output offset zeroing with inputs at zero.

B. Log/Antilog Generator

This circuit consists of a 'Black Box' module, used in conjunction with an operational amplifier and associated potentiometers.

The module is a high accuracy, temperature compensated log module utilizing monolithic devices. The operational amplifier features 5 pA bias current, 300 uV Eos Drift ($\pm$ 10^{o} C) allowing Ein of 2mV to 10V, Ios drift of 2 pA allowing full use of the lower current range (100 pA).

The potentiometer consists of: –

(a) R1 – Scale factor K adjust,

(b) R2 – I Ref adjust,

(c) R3 – Amplifier offset adjust.

R1 and R2 are used in setting up the required ranges of operation (see transfer equations).

In the log mode R3 is used to zero the amplifier offset by first zeroing the log input terminal and adjusting R3 for maximum output within the operating range (± 10V). For the ANTILOG MODE, set the antilog input to −10V and adjust R3 for OV output.

C. Vector Generator

This circuit consists of a 'Black Box' module and an offset potentiometer.

The module is calibrated internally for scale factor K = 1.
K can be set to less than 1 by connecting internally between pin SP and output, an external resistor. Offset is adjusted by placing zero on the input and adjusting for zero output.

DIGITAL PANEL

DIGITAL CLOCK CIRCUIT DESCRIPTION

The digital clock utilizes a unijunction transistor relaxation oscillator circuit as the primary generator source. The output pulse is driven into inverters, Q3 and IC1 so giving outputs of P and $\overline{P}$.

The $\overline{P}$ output drives into the JK flip flop IC2, producing the square wave clock pulse outputs, $\overline{CP}$ and CP.

Three modes of operation are available:

1) Run;
2) Stop;
3) Clear.

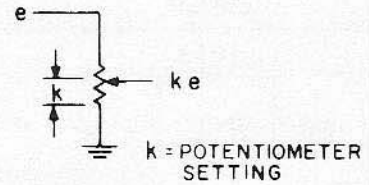
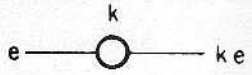
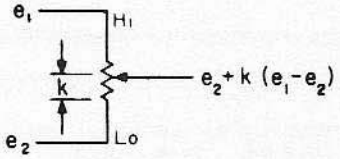
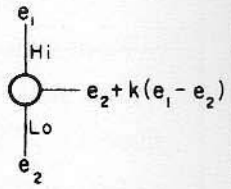
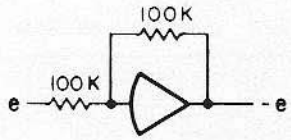
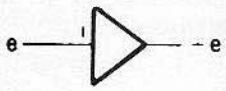
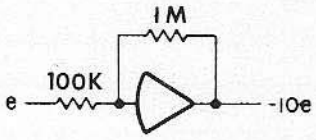
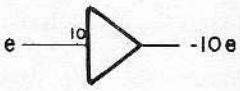
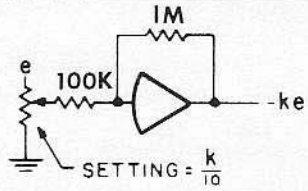
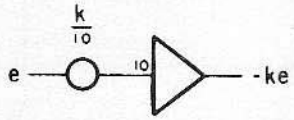
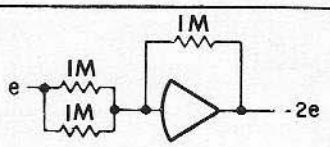
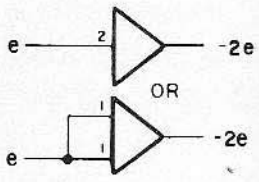
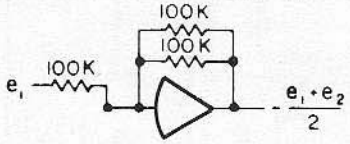
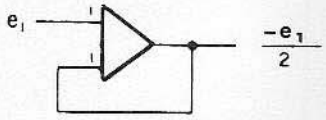
The stop and clear Modes can be controlled mechanically, through the Pushbutton switches, or electronically by applying '0' levels to the patchable inputs.

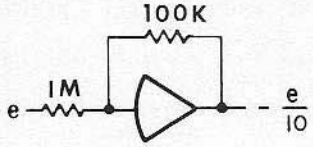
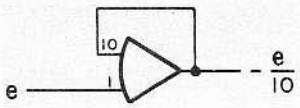
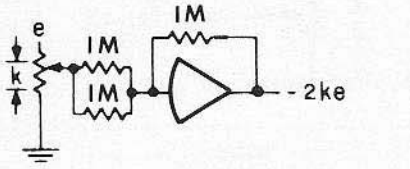
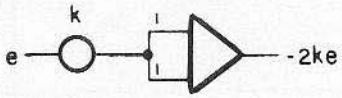
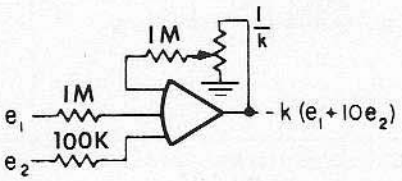
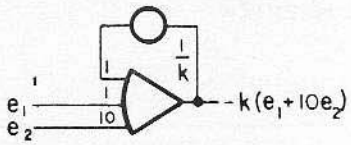
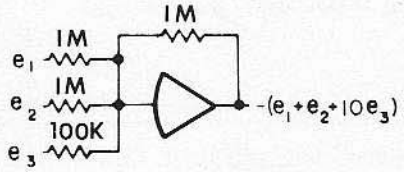
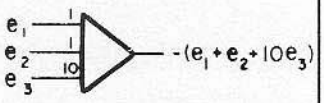
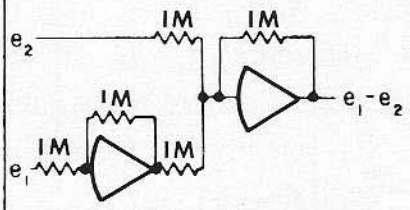
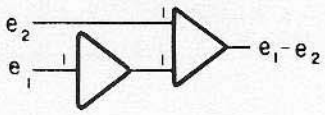
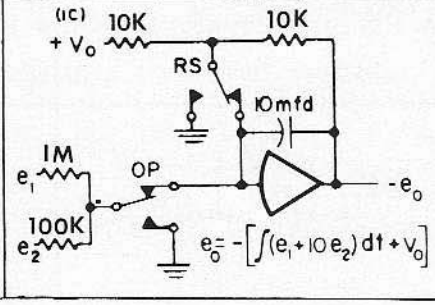
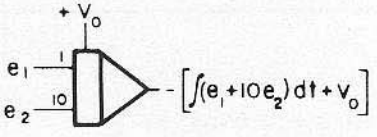
Applying a '0' to the STOP input causes inversion, switches Q2, shorting the oscillator capacitors and stopping the generator; pushing the stop button causes the same effect.

Applying a '0' to the RESET input causes inversion and produces a '1' at $\overline{R}$. This is again inverted to give a '0' at R. Pushing the clear button causes the same effect.

External capacitors may be connected to the oscillator if required, to give any frequency less than the fastest available.

SIMPLE CIRCUITS USING AMPLIFIERS AND POTENTIOMETERS

CIRCUIT DESCRIPTION	CIRCUIT	PROGRAMMING SYMBOL
1. GROUNDED POTENTIOMETER		
2. UNGROUNDED POTENTIOMETER		
3. INVERTER		
4. MULTIPLICATION BY -10		
5. MULTIPLICATION BY -k for $1 \leq k \leq 10$ (for $k < 1$ use circuit 1 feeding circuit 3)		
6. MULTIPLICATION BY 2		
7. MULTIPLICATION BY $\frac{1}{2}$		

CIRCUIT DESCRIPTION	CIRCUIT	PROGRAMMING
8. MULTIPLICATION BY $\frac{1}{10}$		
9. MULTIPLICATION BY AN ARBITRARY VALUE		 $0<k<1.0$
		 $1<k$
10. ADDITION		
11. SUBTRACTION		
12. INTEGRATION		

APPENDIX 1

UNIT SCALING

The process of scaling an analog computer circuit is simplified if the reference voltage of the computer is used as a unit for measuring amplifier outputs. On a ten-volt computer, such as the 180, this means that one unit is defined to be equal to ten volts; all signals, when measured in units, will be $\leqslant$ 1.0000 in magnitude.

There are a number of advantages to such an approach. One of the most obvious (but not the most important) is the fact that the DVM reads in units (when reference voltage is measured on the DVM, the result is +1.0000). This location of the decimal point is determined by the fact that the DVM is used for pot-setting as well as amplifier readout, and pot-setting must be $\leqslant$ 1.0000 in magnitude. If reference voltage is used as the unit of measurement, then amplifier outputs are also $\leqslant$ 1.0000 in magnitude. Hence the decimal point is correctly located in all cases.

The relation between a problem variable and the corresponding computer variable becomes somewhat simpler in terms of unit scaling. For example, if a problem variable P has a maximum value of 50 lbs, then the corresponding computer variable is simply (P/50), which has a maximum value of one. In unit scaling, every computer variable is simply the ratio of the corresponding problem variable to its maximum value.

If the scaling is done in volts, then the computer variable is ten times the ratio of the problem variable to its maximum value. Thus, if P $\leqslant$ 50 lbs, then the computer variable would be (P/5). On a hundred-volt computer, the computer variable would be (2P). This points out another advantage of the "unit scaling" technique — it is machine-independent: the scaled variable would be (P/50) on either machine.

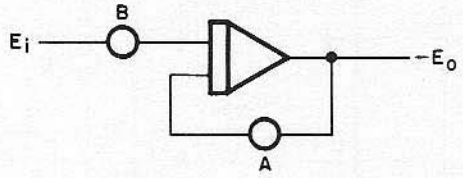
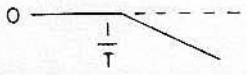
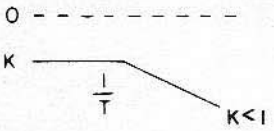
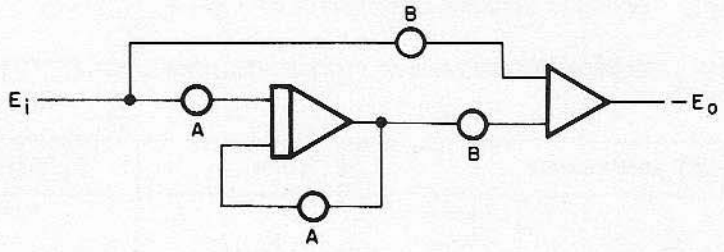
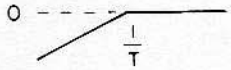
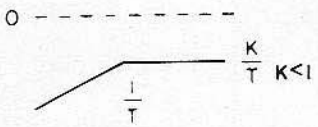
Probably the greatest advantage of unit scaling is the way it simplifies the scaling of non-linear circuits. For example, the product of two variables that are ≤ 1 in magnitude will also be ≤ 1 in magnitude. If a multiplier has scale inputs X and Y ($-1 \leq X \leq 1$, $-1 \leq Y \leq 1$) then the output will simply be the product XY ($-1 \leq XY \leq 1$). If scaled in volts, the output would be XY/10 or XY/100, depending on reference voltage of the machine. Similarly, expressions for square, square root, log exponential, and trigonometric functions are generally simpler when expressed in terms of units.

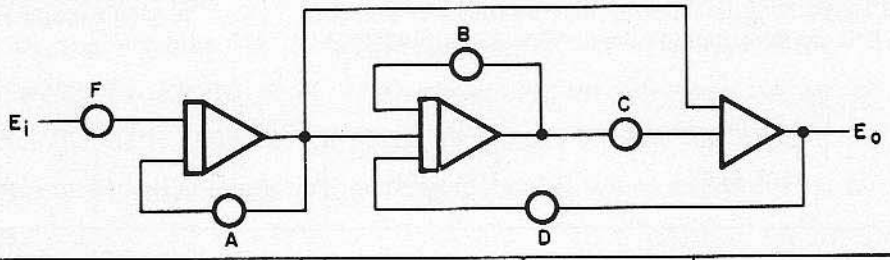
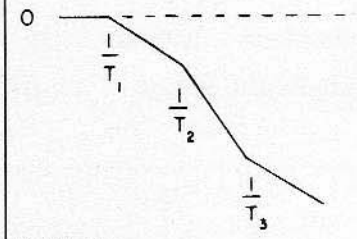
A more complete description of the unit scaling technique is given in Chapter 3 of the Handbook of Analog Computation, available from EAI.

APPENDIX 2

TRANSFER FUNCTION SIMULATION

(1) The following table contains examples of amplifier circuits for simulating transfer functions . A more complete listing may be found in Jackson, A.S., "Analog Computation", McGraw-Hill Book Company, Inc., New York, 1960.

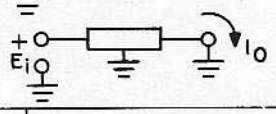
NO.	BODE PLOT	TRANSFER FUNCTION E_o/E_i	TIME CONSTANTS	GAINS
				
1		$\frac{1}{1+Tp}$	$T = \frac{1}{A}$	$A = B = \frac{1}{T}$
2		$\frac{K}{1+Tp}$	$T = \frac{1}{A}$ $K = \frac{B}{A}$	$A = \frac{1}{T}$ $B = \frac{K}{T}$
				
3		$\frac{Tp}{1+Tp}$	$T = \frac{1}{A}$	$A = \frac{1}{T}$ $B = 1$
4		$\frac{Kp}{1+Tp}$	$T = \frac{1}{A}$ $K = \frac{B}{A}$	$A = \frac{1}{T}$ $B = \frac{K}{T}$

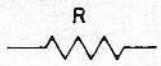
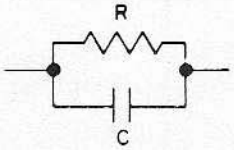
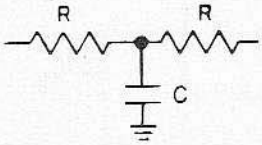
NO.	BODE PLOT	TRANSFER FUNCTION E_o/E_i	TIME CONSTANTS	GAINS
				
5.		$\frac{1+T_3P}{(1+T_1P)(1+T_2P)}$	$T_1 = \frac{1}{A}$ $T_2 = \frac{1}{B-CD}$ $T_3 = \frac{1}{B-C}$	$A = \frac{1}{T_1}$ $B = C + \frac{1}{T_3}$ C = Arbitrary >0 $D = \frac{1}{C}\left(\frac{1}{T_3} - \frac{1}{T_2}\right) + 1$ $F = \frac{T_3}{T_1 T_2}$

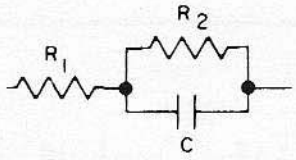
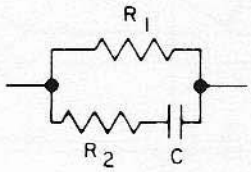
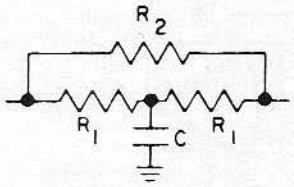
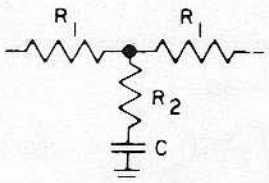
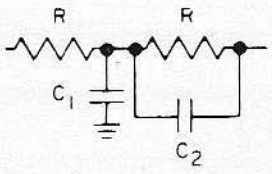
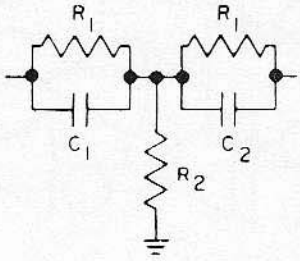
(2) The following table contains the short-circuit admittance and component values for some useful networks for simulating transfer functions. A more extensive listing may be found in Jackson, A.S., "Analog Computation", and Fifer, S. "Analog Computation". (See Bibliography.)

NOTE

The short-circuit admittance of a two or three terminal network represented by 

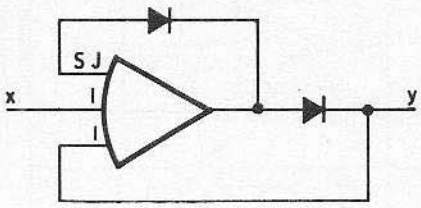
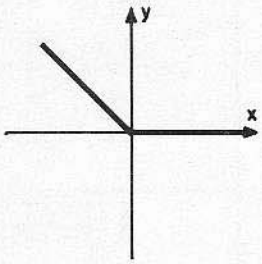
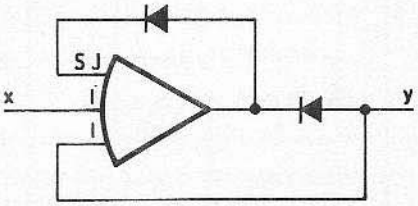
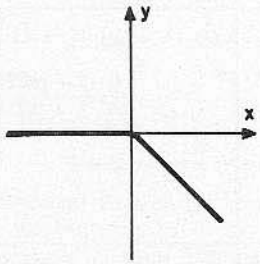
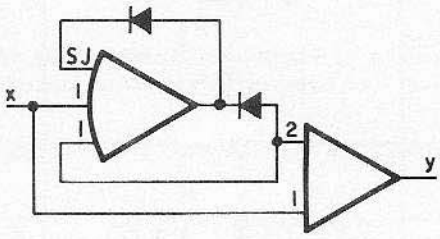
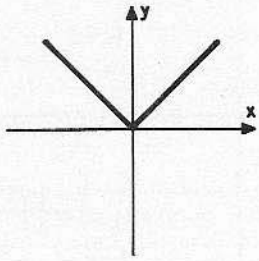
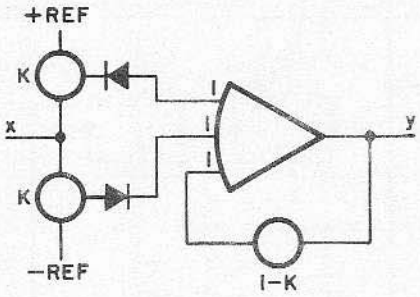
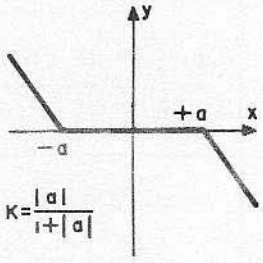
is given by the ratio of $I_o(P)/E_i(P)$ *from* 

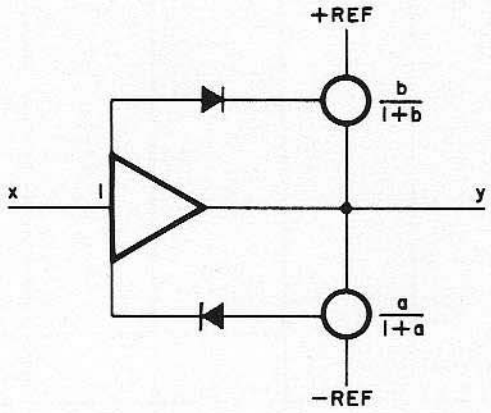
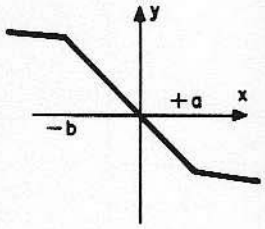
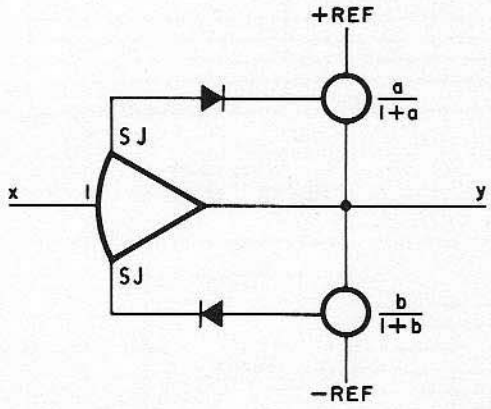
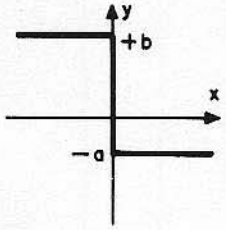
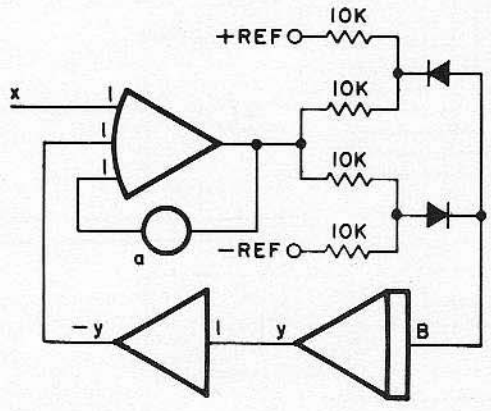
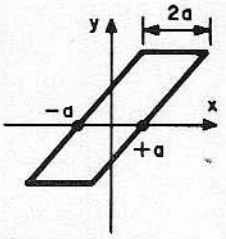
NO.	SHORT-CKT ADMITTANCE	NETWORK	PARAMETERS
1.	$\frac{1}{A}$		A = R
2.	$\frac{1 + pT}{A}$		A = R T = RC
3.	$\frac{1}{A(1 + pT)}$		A = 2R $T = \frac{RC}{2}$

NO.	SHORT-CKT ADMITTANCE	NETWORK	
4.	$\frac{1}{A}\left[\frac{1+pT}{1+p\theta T}\right]$ $\theta < 1$		$A = R_1 + R_2$ $T = R_2 C$ $\theta = \frac{R_1}{R_1 + R_2}$
5.	$\frac{1}{A}\left[\frac{1+pT}{1+p\theta T}\right]$ $\theta < 1$		$A = R_1$ $T = (R_1 + R_2)\, C$ $\theta = \frac{R_2}{R_1 + R_2}$
6.	$\frac{1}{A}\,\frac{1+p\theta T}{1+pT}$ $\theta < 1$		$A = \frac{2R_1 R_2}{2R_1 + R_2}$ $T = \frac{R_1 C}{2}$ $\theta = \frac{2R_1}{2R_1 + R_2}$
7.	$\frac{1}{A}\,\frac{1+p\theta T}{1+pT}$ $\theta < 1$		$A = 2R_1$ $T = \left[R_2 + \frac{R_1}{2}\right] C$ $\theta = \frac{2R_2}{2R_2 + R_1}$
8.	$\frac{1}{A}\,\frac{1+p\theta T}{1+pT}$ $\theta < 1$		$A = 2R$ $T = \frac{R}{2}(C_1 + C_2)$ $\theta = \frac{2C_2}{C_1 + C_2}$
9.	$\frac{1}{A}\left[\frac{(1+pT_1)(1+pT_3)}{(1+pT_2)}\right]$ $T_1 > T_2 > T_3$		$A = 2R_1 + \frac{R_1^2}{R_2}$ $T_1 = R_1 C_1$ $T_2 = \left[\frac{R_1 R_2}{R_1 + 2R_2}\right](C_1 + C_2)$ $T_3 = R_1 C_2$

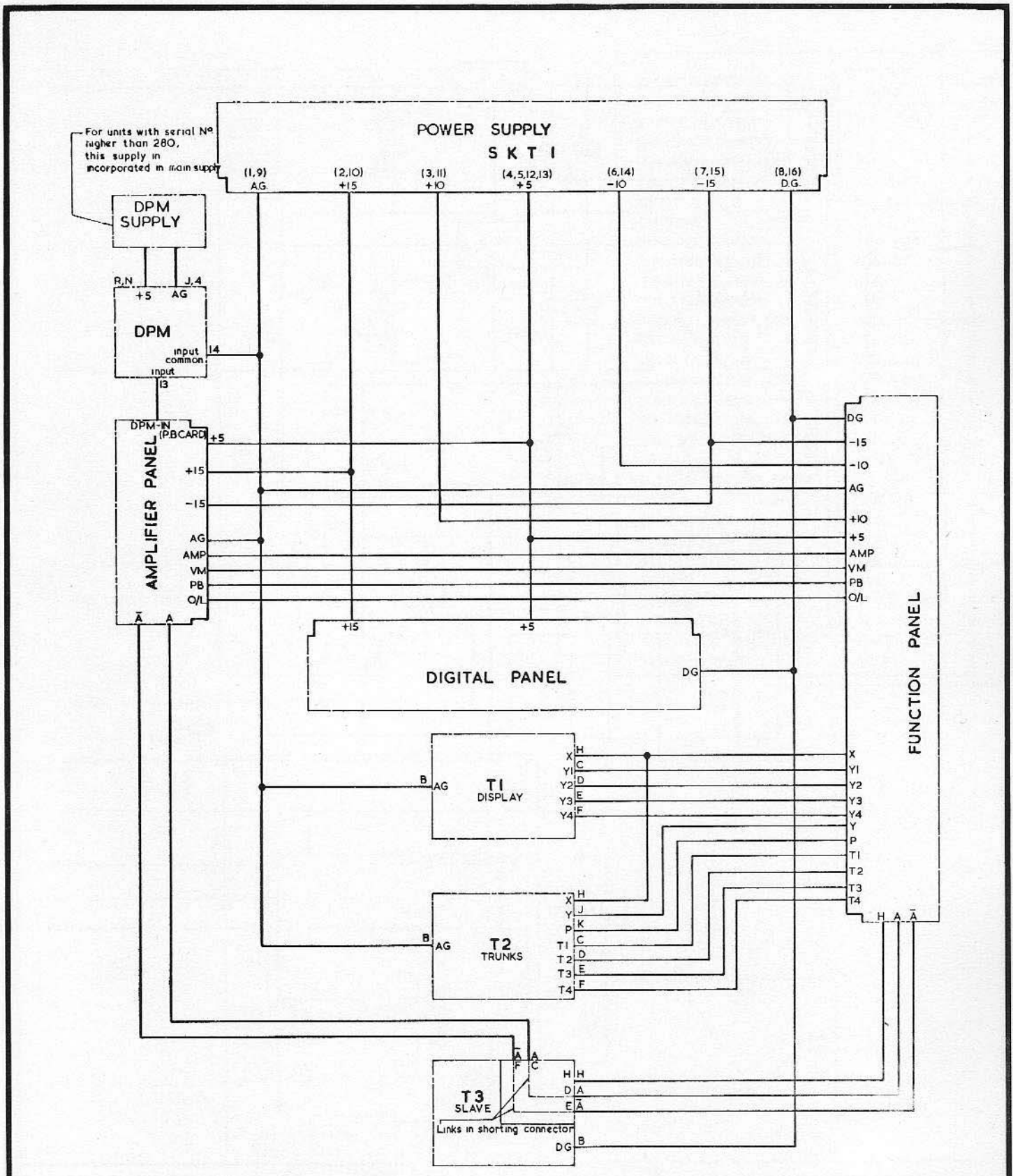
APPENDIX 3

REPRESENTATION OF CONSTRAINTS AND NONLINEARITIES

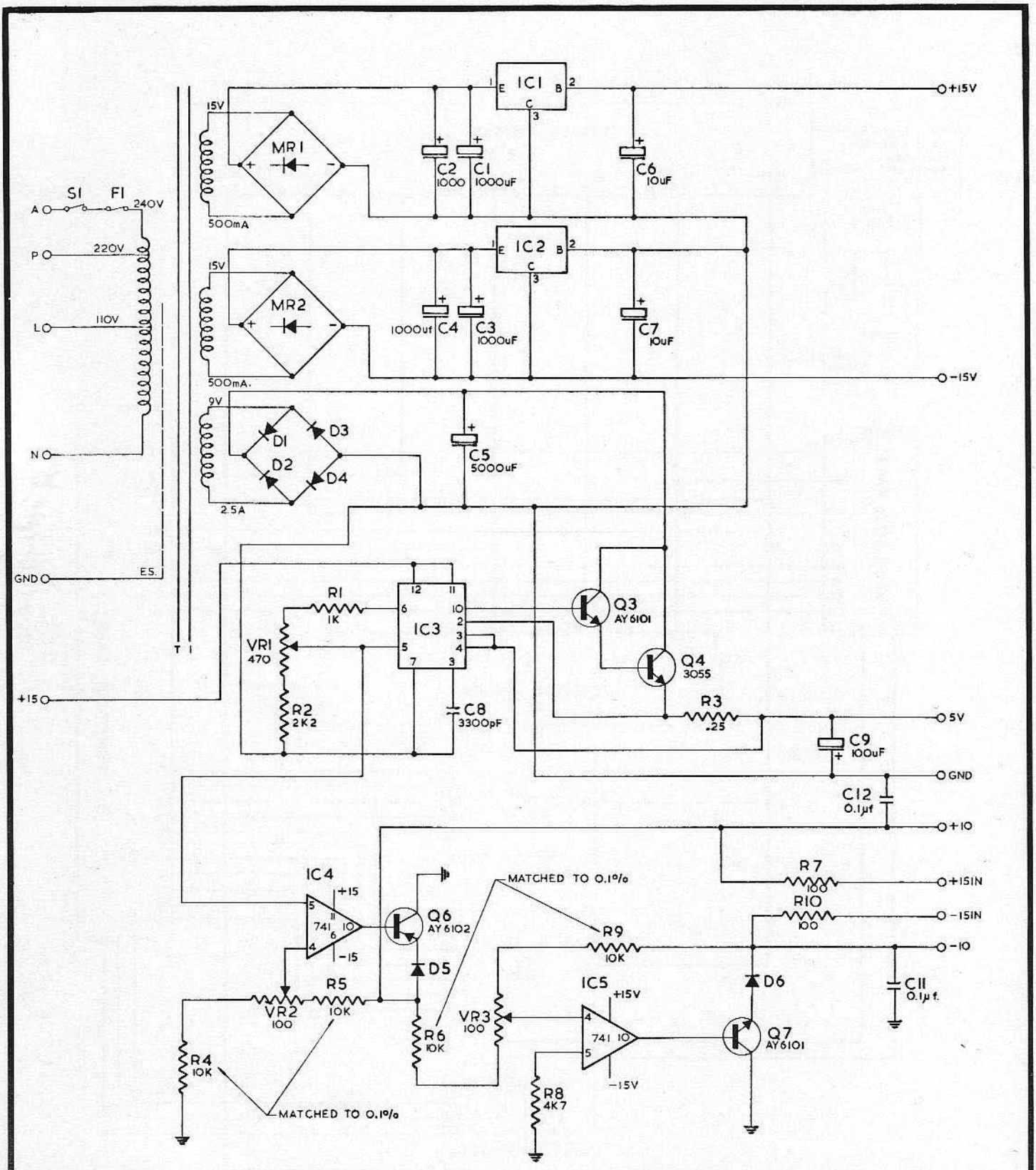
1. HARD ZERO LIMIT		
2. HARD ZERO LIMIT		
3. ABSOLUTE VALUE	 FOR $-\|x\|$, REVERSE THE DIODES	
4. DEAD SPACE		

5. LIMITER		
6. BANG−BANG CIRCUIT (CAN BE USED AS COMPARATOR		
7. BACKLASH (HYSTERESIS)		

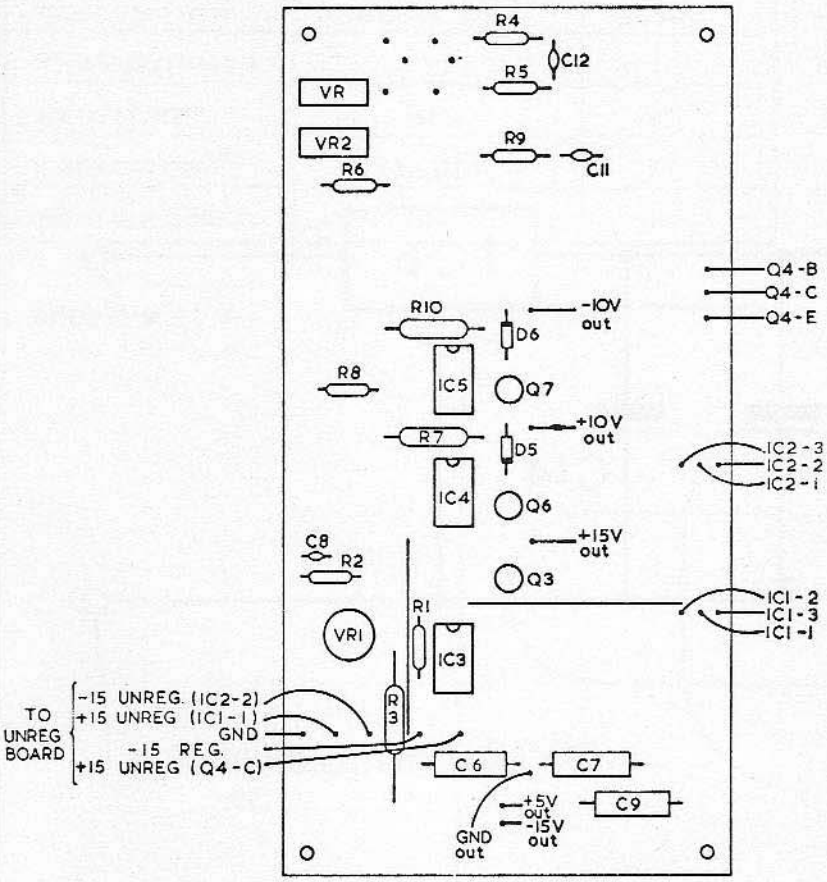
CIRCUIT DIAGRAMS



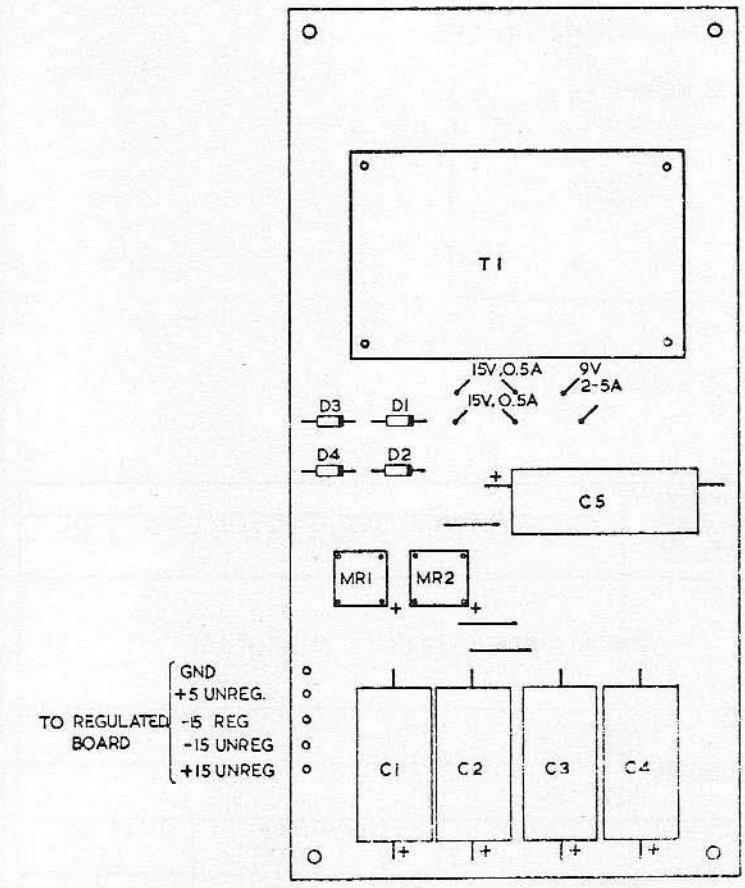
ELECTRONIC ASSOCIATES PTY. LTD.			
TITLE: POWER HARNESS PANEL & TRUNK CONNECTIONS			
NO. 180-54			
PROJECT EAI-180			
DRAWN M.P.	DATE 3.3.72.	DESIGNER G.F.G.	SHEET NO. 3



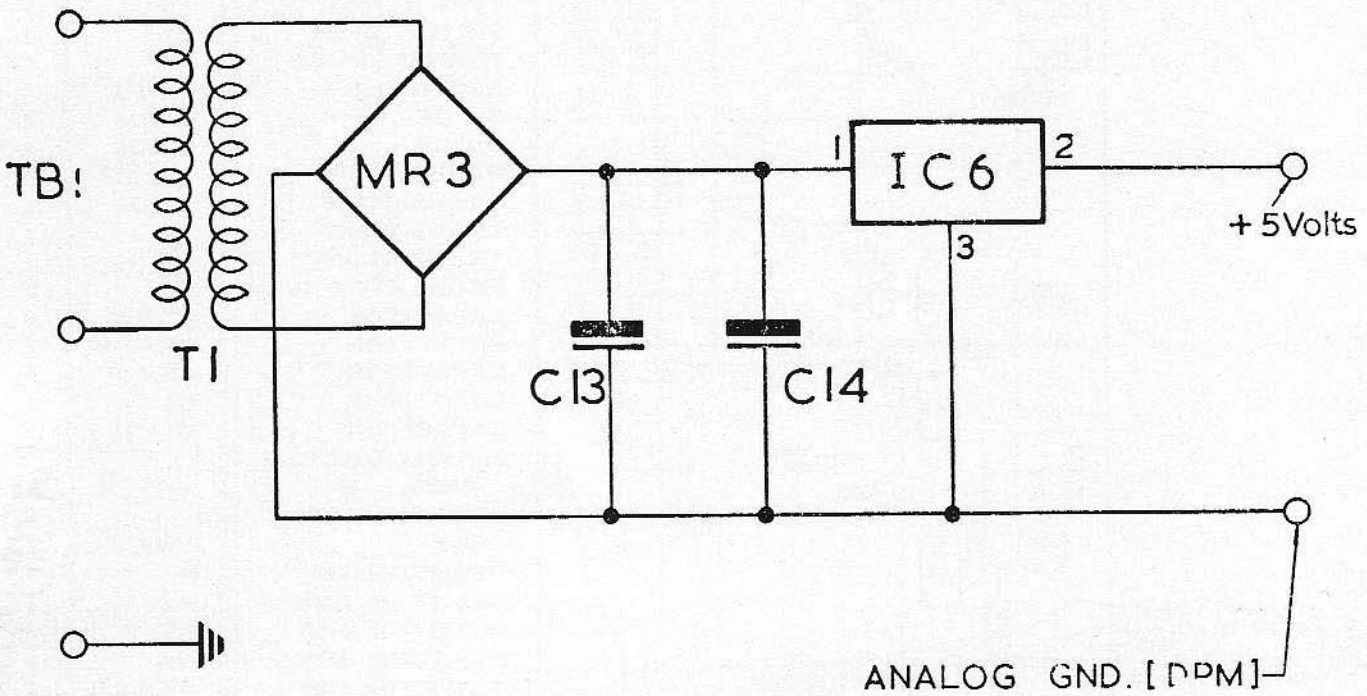
ELECTRONIC ASSOCIATES PTY. LTD.				
TITLE: POWER SUPPLY AND REGULATOR CIRCUIT DIAGRAM				
NO. 180-36/47A				
PROJECT EAI-180				
DRAWN M.P.	DATE 7.8.72	DESIGNER G.F.G.	SHEET NO. 1A	



DESCRIPTION	CIRCUIT REF.	QUAN
FUSE 1 AMP	F1	1
SWITCH DPDT	S1	1
TRANSFORMER	T1	1
RECTIFIER	MR1,2	2
DIODE	D1-D4	4
DIODE	D5,D6	2
REGULATOR	IC1,IC2	2
TRANSISTOR	Q3,Q7	2
TRANSISTOR	Q4	1
TRANSISTOR	Q6	1
REGULATOR IC	IC3	2
CAPACITOR	C1-C4	4
CAPACITOR	C5,C10	2
CAPACITOR	C6,7,9	3
CAPACITOR	C8	1
CAPACITOR	C11,12	2
POTENTIOMETER 470	VR1	1
POTENTIOMETER 100	VR2,3	2
RESISTOR 1K	R1	1
RESISTOR 2.2K	R2	1
RESISTOR 0-25	R3	1
RESISTOR 4.7K	R8	1
RESISTOR 10K	R4,5,6,9	4
RESISTOR 100	R7,10	2
SOCKET OUTPUT	SKT1	1
MAINS PLUG	PL1	1



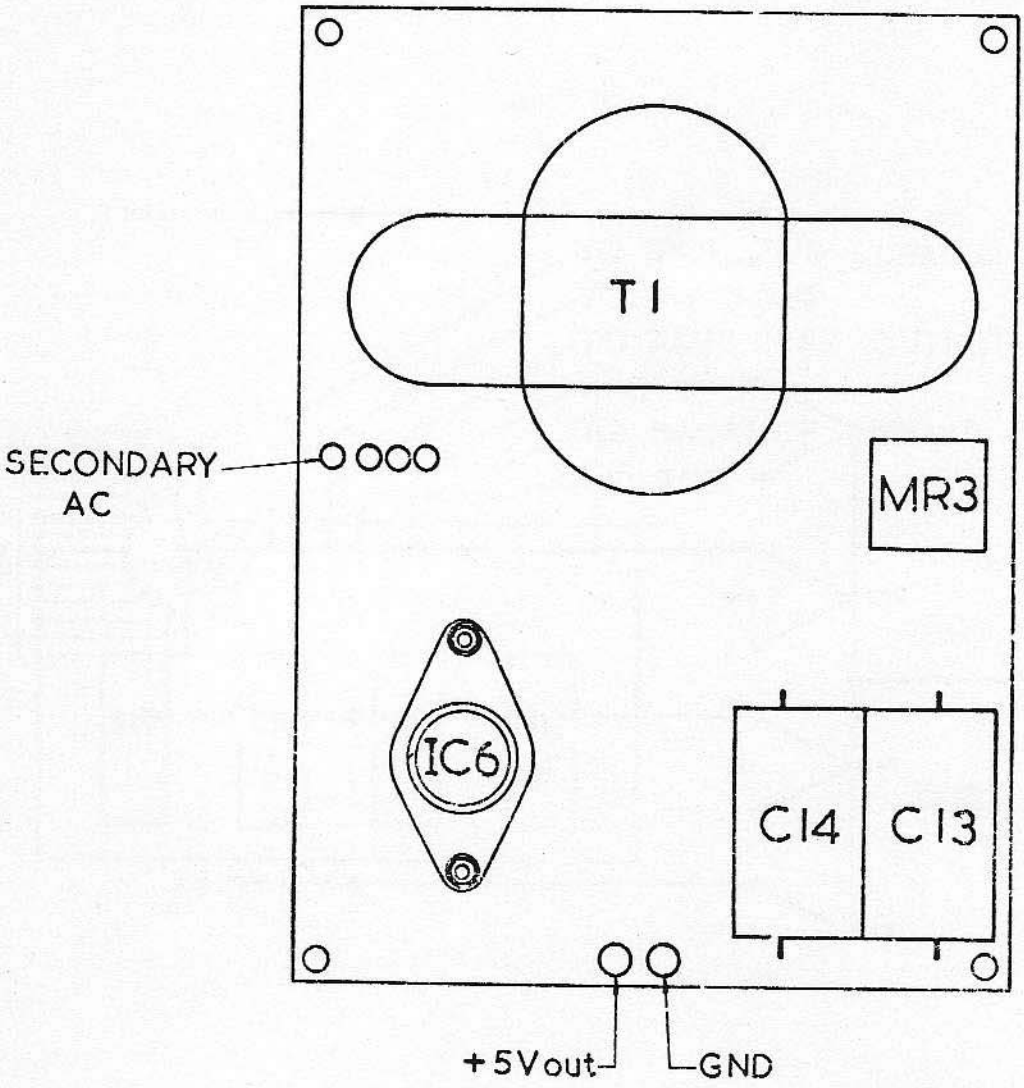
	ELECTRONIC ASSOCIATES PTY. LTD.
TITLE	POWER SUPPLY MOD 180-36
NO.	180-36/47D
PROJECT	EAI-180
DRAWN M.P. / DATE 21.3.72. / DESIGNER G.F.G. / SHEET NO. 1B	



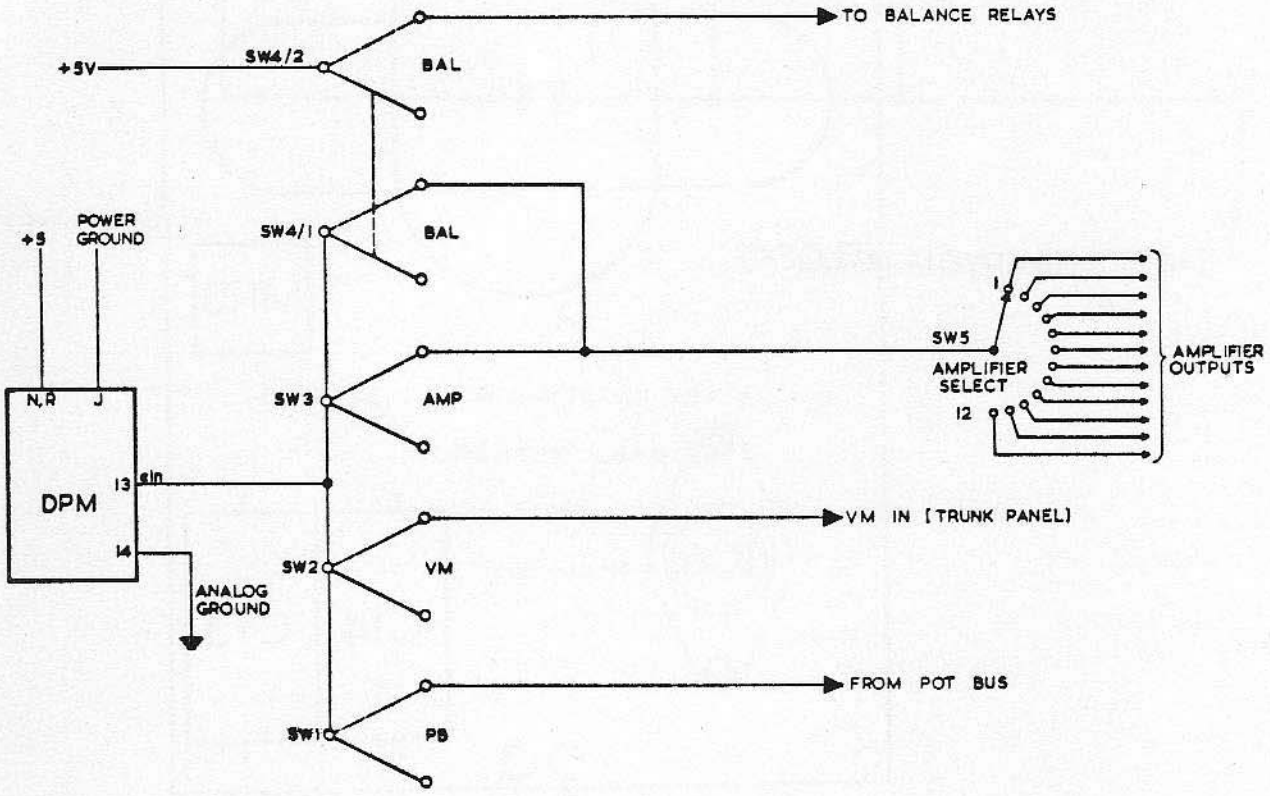
NOTE: FOR UNITS OF SERIAL NO.
GREATER THAN 280
THIS SUPPLY IS INCORPORATED
IN THE MAIN SUPPLY.

ELECTRONIC ASSOCIATES PTY. LTD.			
TITLE: DPM SUPPLY CIRCUIT DIAGRAM			
NO. 180-57A			
PROJECT EAI-180			
DRAWN	DATE 6.72.	DESIGNER G.F.G.	SHEET NO. 2A

PARTS		
DESCRIPTION	CIRCUIT REF.	QUAN
TRANSFORMER	T1	1
RECTIFIER	MR3	1
CAPACITOR	C13, C14	2
REGULATOR	IC6	1

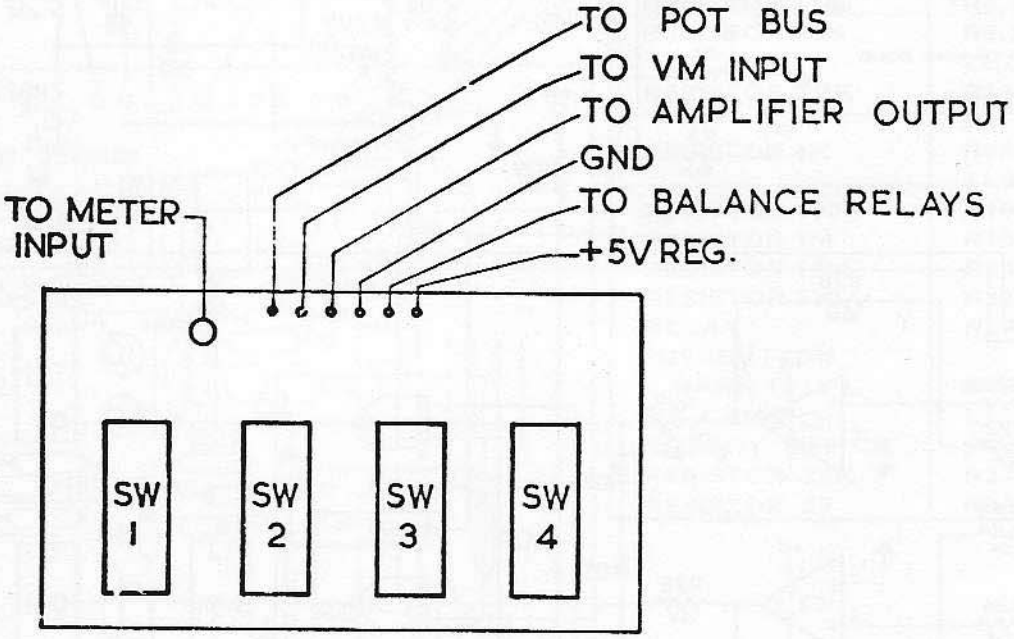


ELECTRONIC ASSOCIATES PTY. LTD.			
TITLE: DPM. POWER SUPPLY COMPONENT LAYOUT			
NO. 180-57D			
PROJECT EAI-180			
DRAWN M.P.	DATE 6.72.	DESIGNER G.F.G.	SHEET NO. 2B

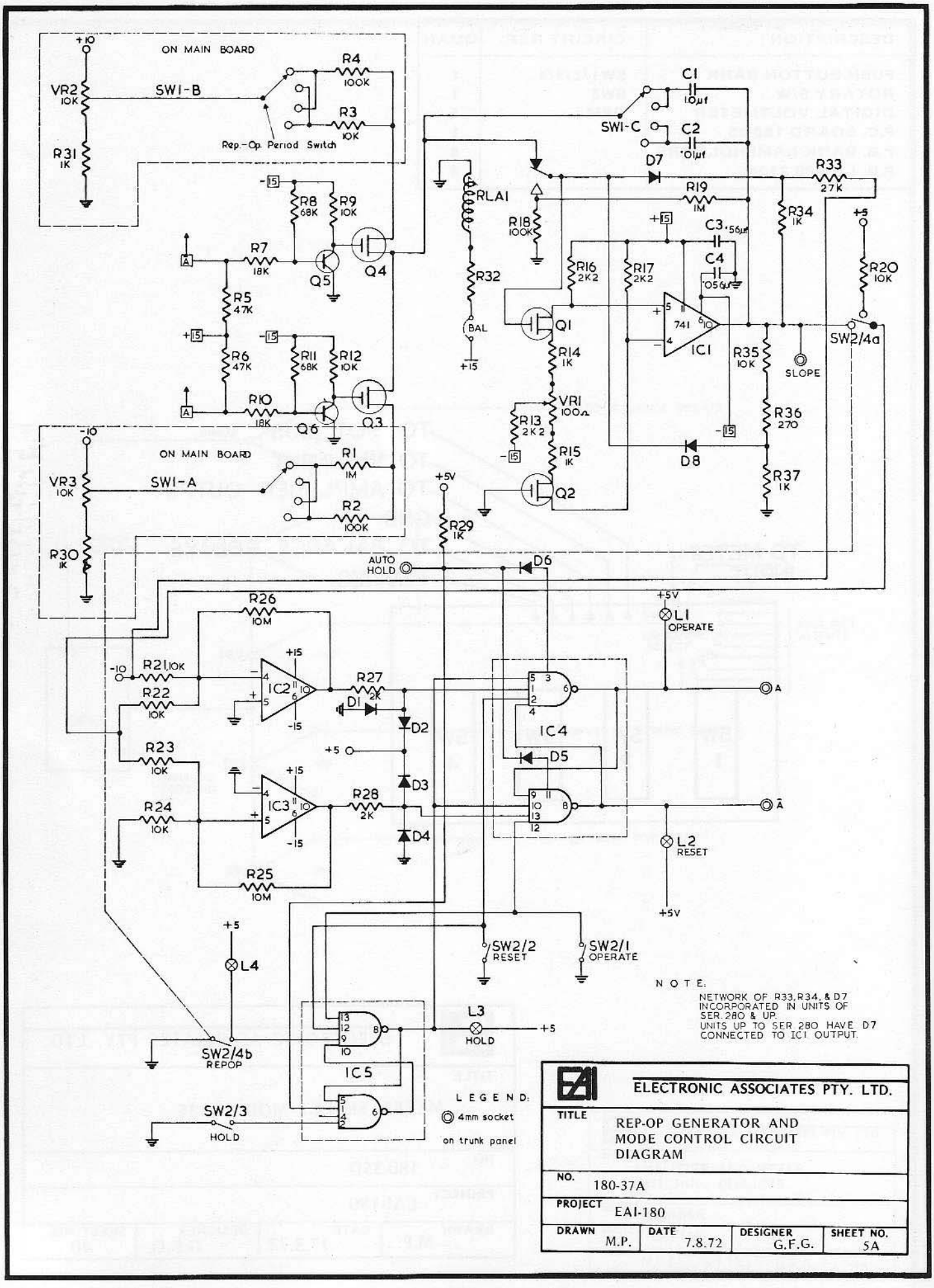


ELECTRONIC ASSOCIATES PTY. LTD.				
TITLE: AMPLIFIER AND METER SWITCHING CIRCUITS				
NO. 180-56A				
PROJECT EAI-180				
DRAWN M.P.	DATE 6.3.72.	DESIGNER G.F.G.	SHEET NO. 4A	

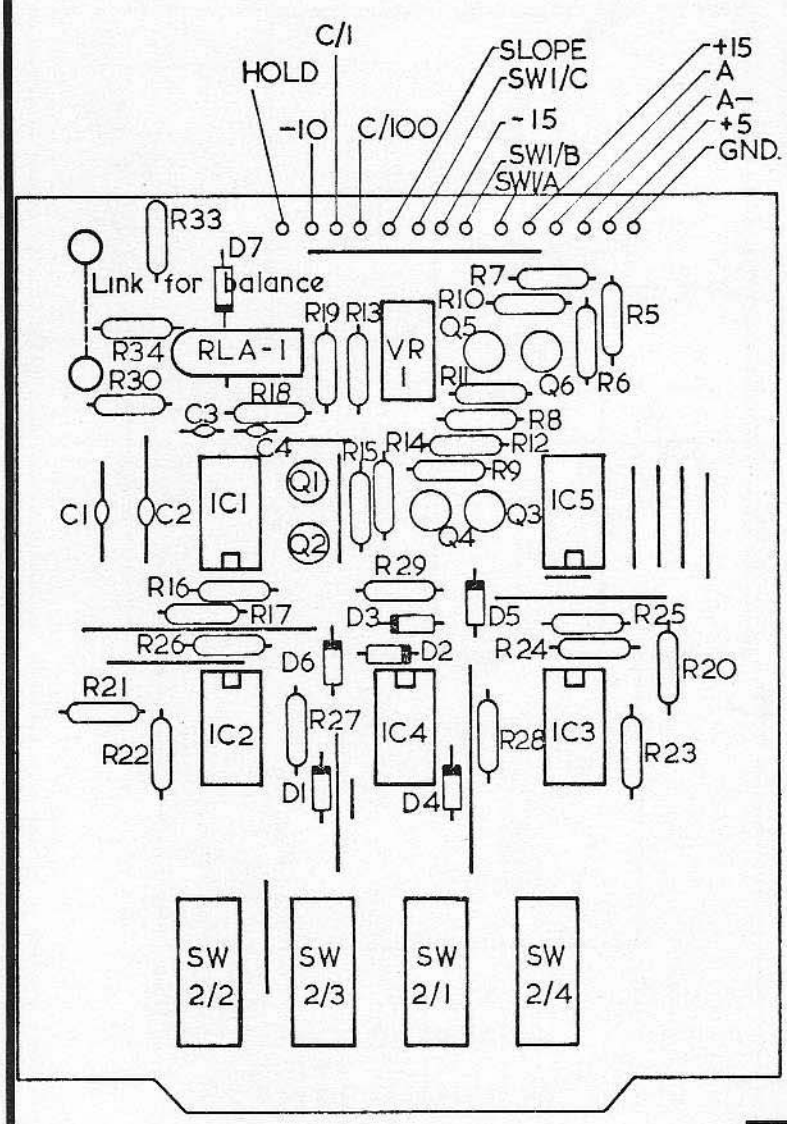
DESCRIPTION	CIRCUIT REF.	QUAN
PUSH BUTTON BANK	SW1/2/3/4	1
ROTARY S/W	SW5	1
DIGITAL VOLTMETER	DPM	1
P.C. BOARD 180-35		1
P.B. BANK LAMPHOLDERS		4
P.B. LAMPS 2306		4



ELECTRONIC ASSOCIATES PTY. LTD.			
TITLE: METER SELECT MOD 180-35			
NO. 180-35D			
PROJECT EAI-180			
DRAWN M.P.	DATE 17.3.72.	DESIGNER G.F.G.	SHEET NO. 4B



ELECTRONIC ASSOCIATES PTY. LTD.			
TITLE: REP-OP GENERATOR AND MODE CONTROL CIRCUIT DIAGRAM			
NO. 180-37A			
PROJECT EAI-180			
DRAWN M.P.	DATE 7.8.72	DESIGNER G.F.G.	SHEET NO. 5A



DESCRIPTION	CIRCUIT REF.	QUAN
OP AMP IC	IC1,2,3	3
DUAL GATE IC	IC4,5	2
TRANSISTOR F.E.T.	Q1,2,3,4	4
TRANSISTOR	Q5,Q6	2
DIODE	D1-D7	7
CAPACITOR	C1	1
CAPACITOR	C2	1
CAPACITOR	C3,C4	2
POTENTIOMETER 10K	VR2,VR3	2
POTENTIOMETER 100	VR1	1
RESISTOR 1M	R1	1
RESISTOR 100K	R2,R4	2
RESISTOR 10K	R3	1
RESISTOR 47K	R5,6	2
RESISTOR 18K	R7,10	2
RESISTOR 68K	R8,11	2
RESISTOR 10K	R9,12,20,21' 22,23,24	7
RESISTOR 2.2K	R13,16,17,27, 28	5
RESISTOR 1K	R14,15,29,30, 31,34	6
RESISTOR 100K	R18	1
RESISTOR 1M	R19	1
RESISTOR 10M	R25,26	2
RESISTOR 330	R32	1
RELAY	RLA1	1
PUSHBUTTON BANK 1233-4	SW2	1
P.B. LAMPS	L1,2,3,4	
ROTARY SWITCH	SW1	1
RESISTOR 27K	R33	1
RESISTOR 27	R36	1

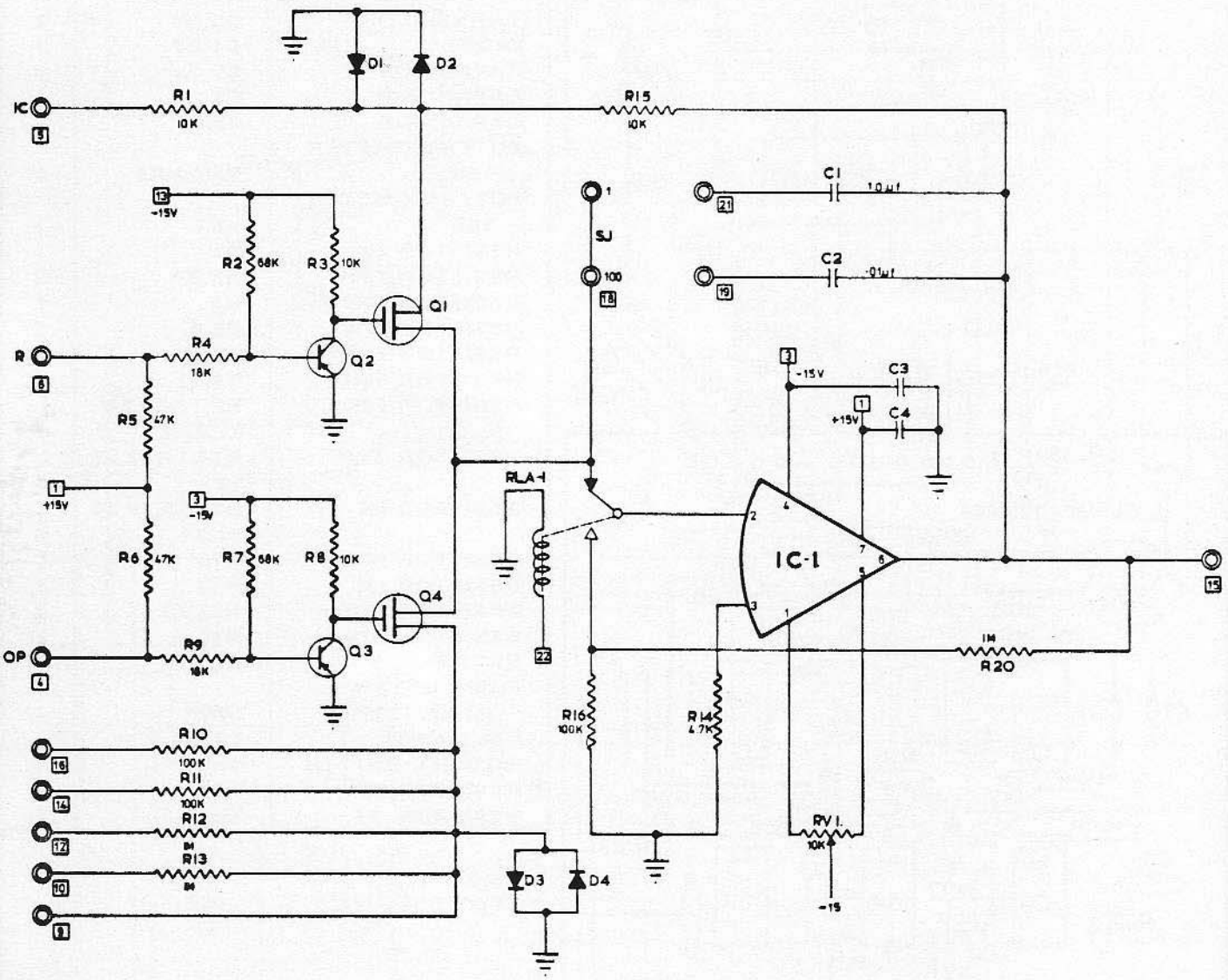
ELECTRONIC ASSOCIATES PTY. LTD.

TITLE: REP-OP GENERATOR AND MODE CONTROL CIRCUIT DIAGRAM

NO. 180-37A

PROJECT EAI-180

DRAWN	DATE	DESIGNER	SHEET NO.
M.P.	9.3.72.	G.F.G.	13



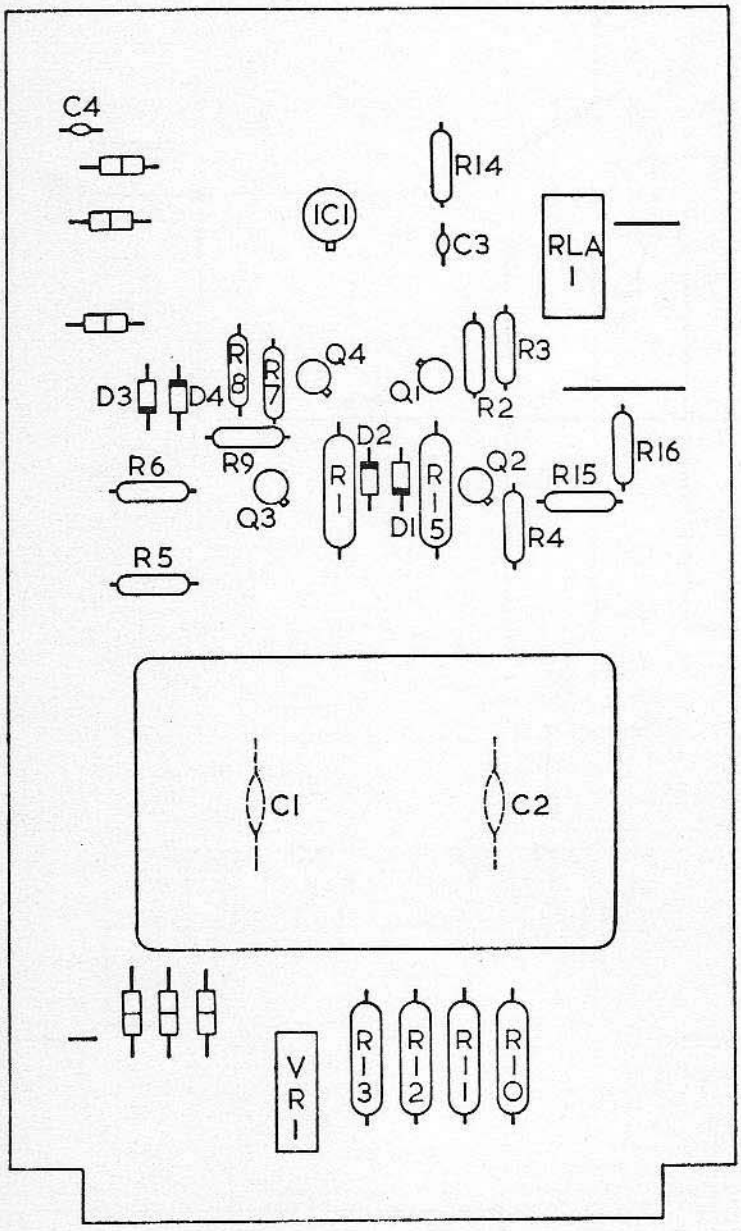
LEGEND:

[2] Pin N° on edge connector

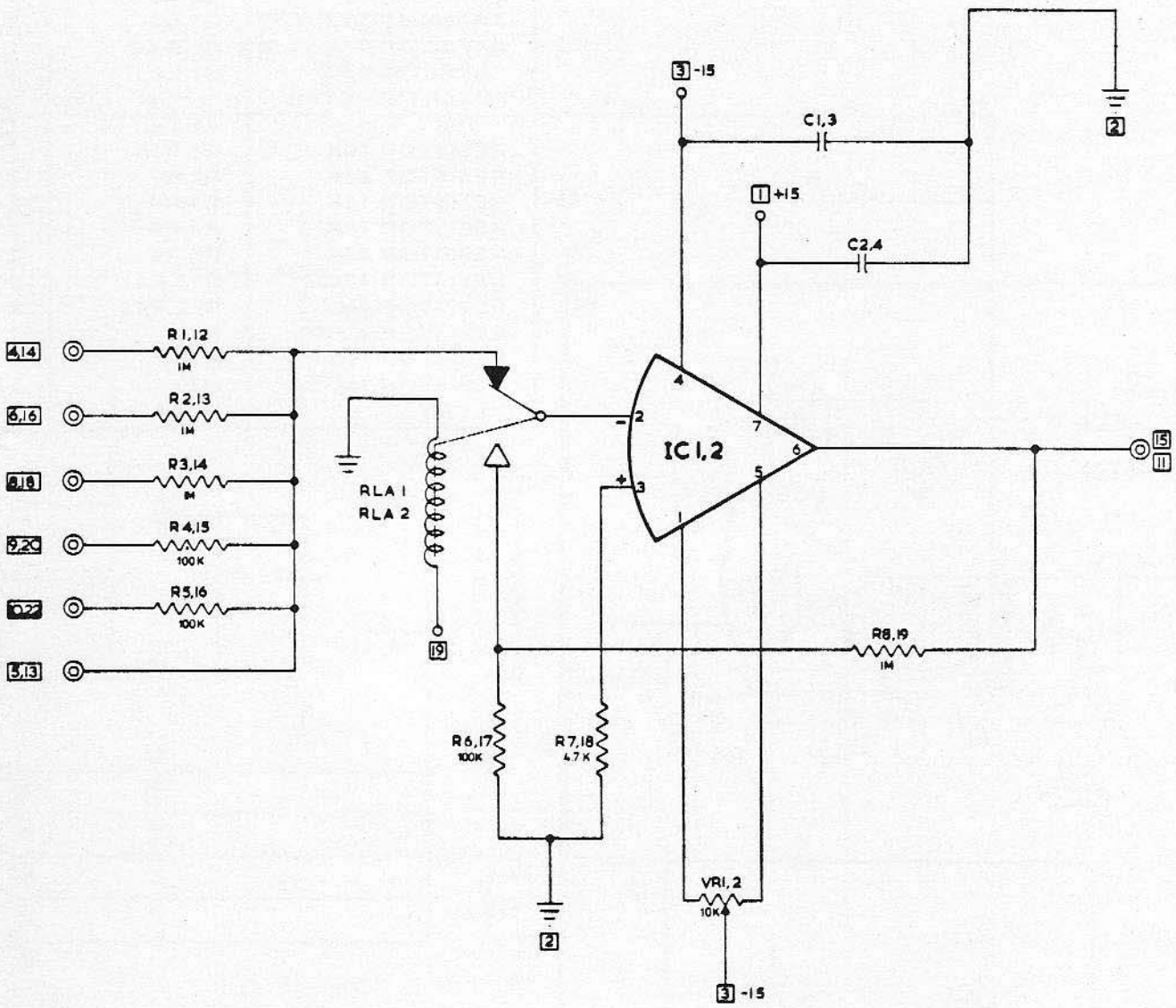
4mm socket on front panel

ELECTRONIC ASSOCIATES PTY. LTD.			
TITLE: INTEGRATOR CIRCUIT DIAGRAM			
NO. 180-32A			
PROJECT EAI-180			
DRAWN M.P.	DATE 7.3.72.	DESIGNER G.F.G.	SHEET NO. 6A

DESCRIPTION	CIRCUIT REF.	QUAN
OP.AMP.IC	IC1	1
DIODE	D1-D4	4
TRANSISTOR	Q2,Q3	2
TRANSISTOR F.E.T.	Q1,Q4	2
CAPACITOR	C1 & C2	1
CAPACITOR	C3,C4	2
POTENTIOMETER 10K	VR1	1
RESISTOR 10K	R1,R15	2
RESISTOR 68K	R2,R7	2
RESISTOR 10K	R3,R8	2
RESISTOR 18K	R4,R9	2
RESISTOR 47K	R5,R6	2
RESISTOR 100K	R10,R11	2
RESISTOR 1M	R12,R13	2
RESISTOR 4.7K	R14	1
RESISTOR 100K	R16	1
RESISTOR 1M	R20	1
RELAY	RLA1	1



ELECTRONIC ASSOCIATES PTY. LTD.				
TITLE: INTEGRATOR MOD 180-32				
NO. 180-32D				
PROJECT EAI-180				
DRAWN M.P.	DATE 17.3.72.	DESIGNER G.F.G.	SHEET NO. 6B	



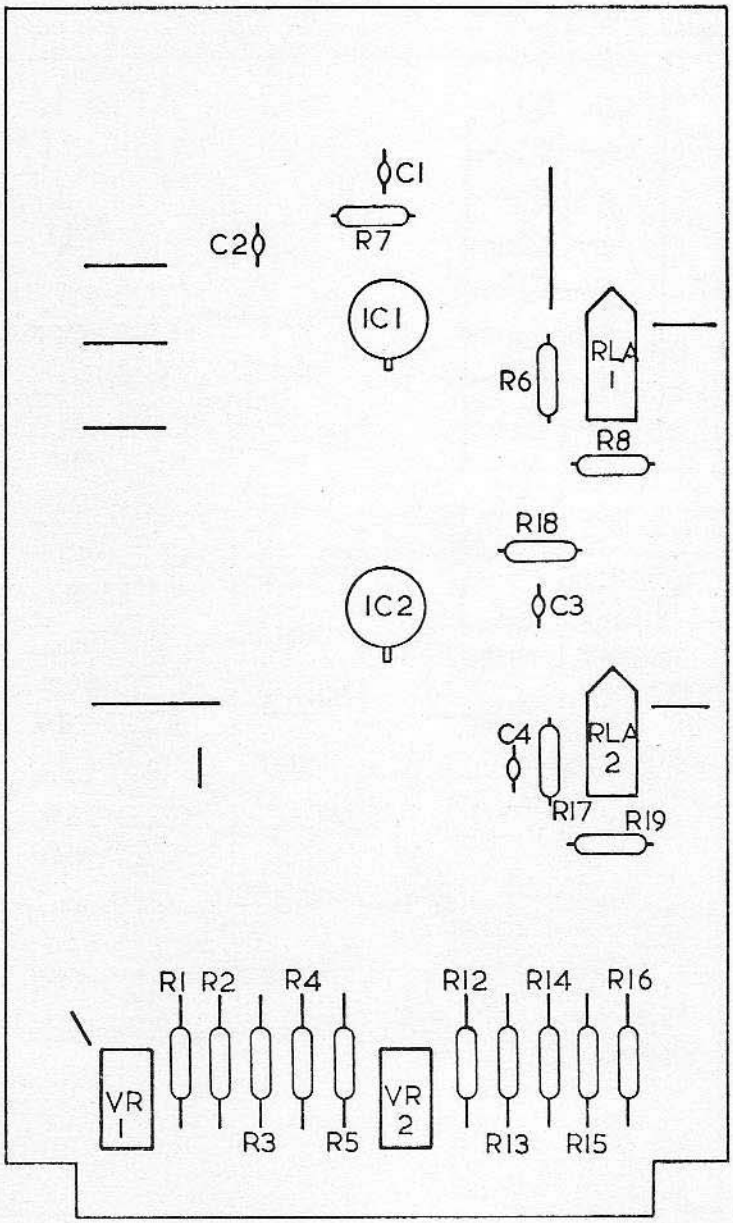
LEGEND:

10 Pin Nº on edge connector

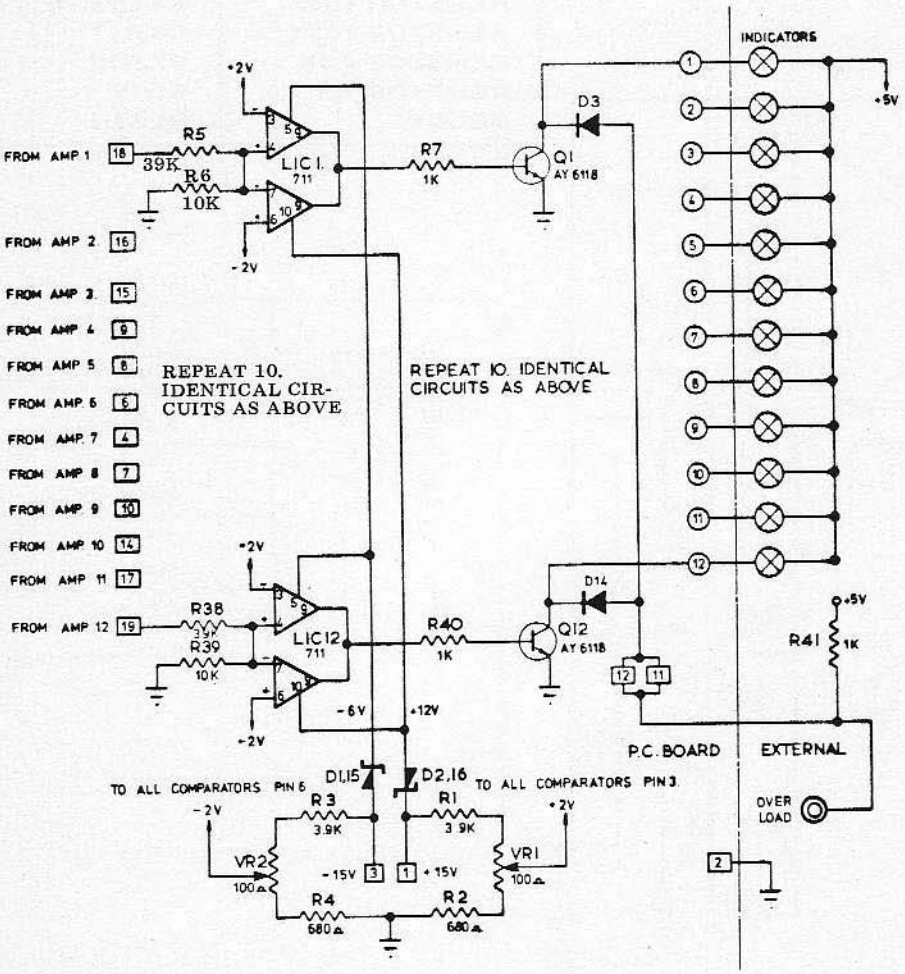
4mm socket on front panel

ELECTRONIC ASSOCIATES PTY. LTD.			
TITLE: DUAL SUMMER CIRCUIT DIAGRAM			
NO. 180-33A			
PROJECT EAI-180			
DRAWN M.P.	DATE 4.3.72.	DESIGNER G.F.G.	SHEET NO. 7A

DESCRIPTION	CIRCUIT REF.	QUAN
OP.AMP.IC	IC1,IC2	2
POTENTIOMETER 10K	VR1,VR2	2
CAPACITORS	C1-C4	4
RESISTOR 1M	R1,2,3,12,13, 14	6
RESISTOR 100K	R4,5,15,16	4
RESISTOR 100K	R6,R17	2
RESISTOR 4.7K	R7,R18	2
RESISTOR 1M	R8,19	2
RELAY	RLA1-2	2



ELECTRONIC ASSOCIATES PTY. LTD.			
TITLE: DUAL SUMMER MOD 180-33			
NO.: 180-33D			
PROJECT: EAI-180			
DRAWN: M.P.	DATE: 20.3.72.	DESIGNER: G.F.G.	SHEET NO.: 7B



LEGEND

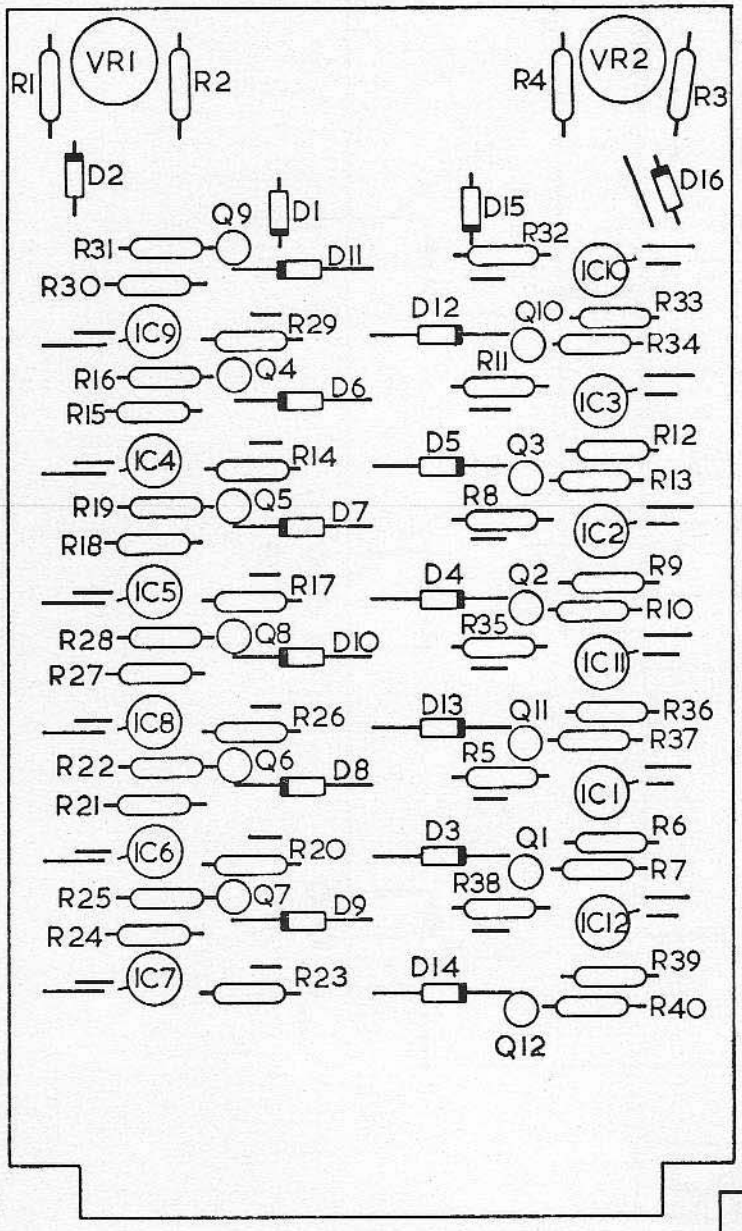
[13] Pin N° on edge connector

(7) Pin N° on AMP plug

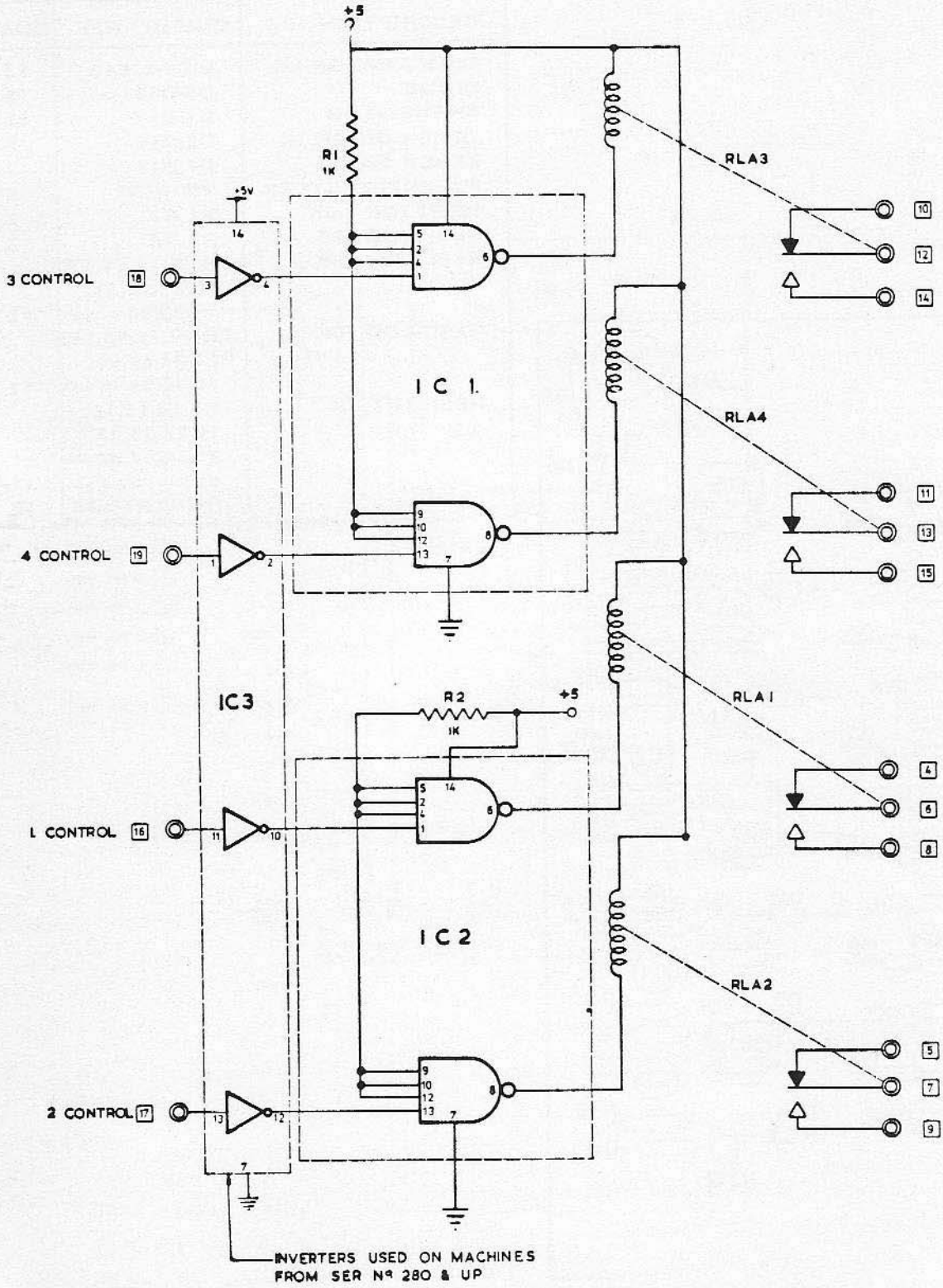
◎ 4mm socket on trunk panel

ELECTRONIC ASSOCIATES PTY. LTD.			
TITLE: OVERLOAD CARD CIRCUIT DIAGRAM			
NO. .180-12A			
PROJECT EAI-180			
DRAWN M.P.	DATE 3.3.72.	DESIGNER G.F.G.	SHEET NO. 8A.

DESCRIPTION	CIRCUIT REF.	QUAN
COMPARATOR I.C	LIC1-LIC12	12
DIODE	D3-D14	12
TRANSISTOR	Q1-Q12	12
ZENER DIODE	D2,D16	2
ZENER DIODE	D1,D15	2
POTENTIOMETERS	VR1,VR2	2
RESISTOR 3-9K	R1,R3	2
RESISTOR 680	R2,R4	2
RESISTOR 39K	R5,8,11,14,17, 20,23,26,29, 32,35,38	12
RESISTOR 10K	R6,9,12,15,18, 21,24,27,30, 33,36,39	12
RESISTOR 1K	R7,10,13,16, 19,22,25,28, 31,34,37,40, 41	12
LAMP	INDICATORS	12



EAI	ELECTRONIC ASSOCIATES PTY. LTD.		
TITLE	OVERLOAD MOD 180-12		
NO.	180-12D		
PROJECT	EAI-180		
DRAWN M.P.	DATE 18.3.72.	DESIGNER G.F.G.	SHEET NO. 8B



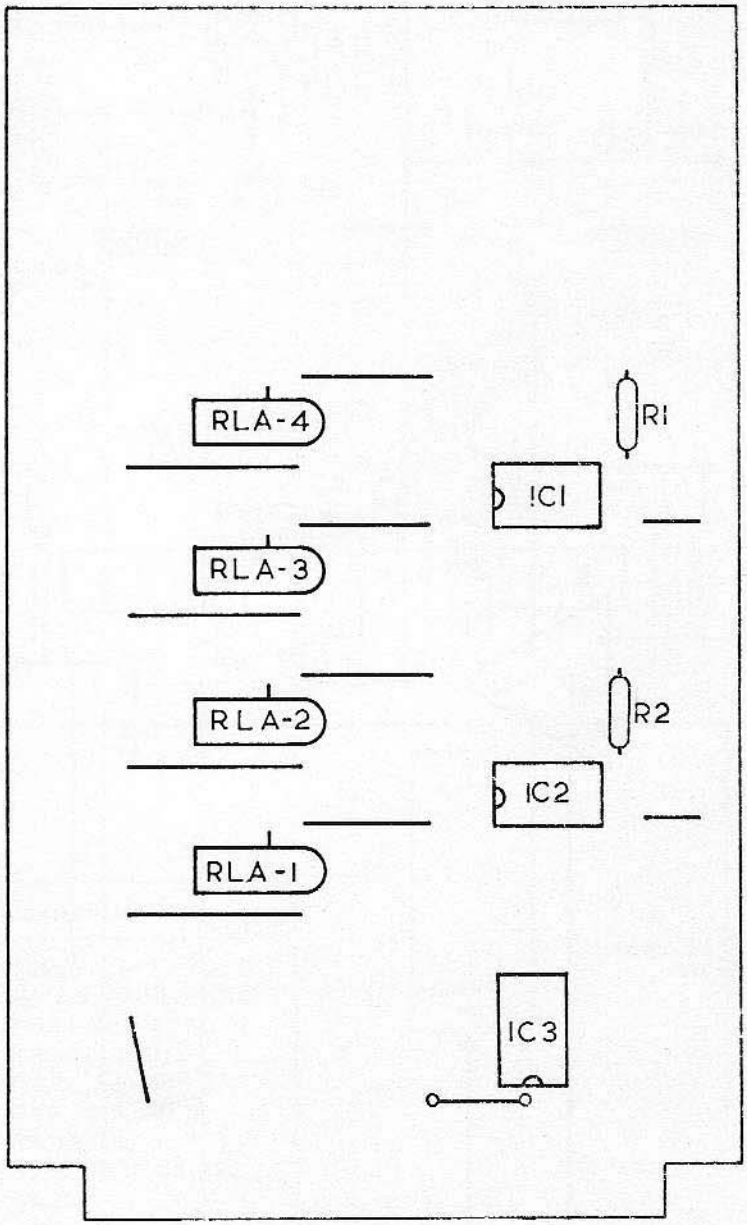
LEGEND:

17 Pin Nº on edge connector

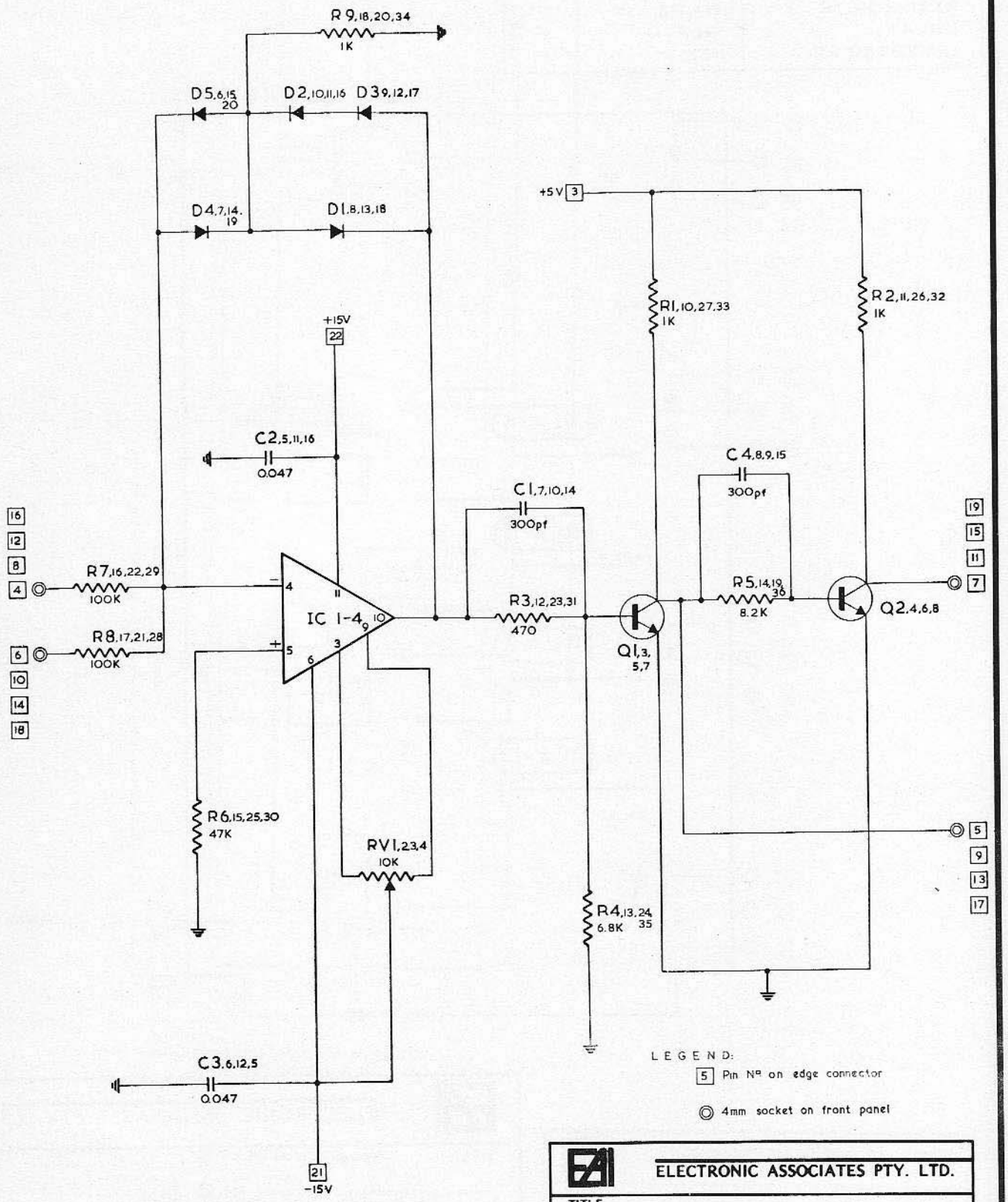
4mm socket on front panel

ELECTRONIC ASSOCIATES PTY. LTD.	
TITLE	QUAD FUNCTION RELAYS
NO.	180-46A
PROJECT	EAI-180
DRAWN M.P. / DATE 8.3.72. / DESIGNER G.F.G. / SHEET NO. 10A	

DESCRIPTION	CIRCUIT REF.	QUAN
DUAL GATE I.C.	IC1,IC2	2
RESISTOR 1K	R1,R2	2
RELAY	RLA1-4	4
INVERTER I.C.	IC3	1



ELECTRONIC ASSOCIATES PTY. LTD.			
TITLE: FUNCTION RELAYS MOD 180-46			
NO. 180-46D			
PROJECT EAI-180			
DRAWN M.P.	DATE 20.3.72.	DESIGNER G.F.G.	SHEET NO. 10B

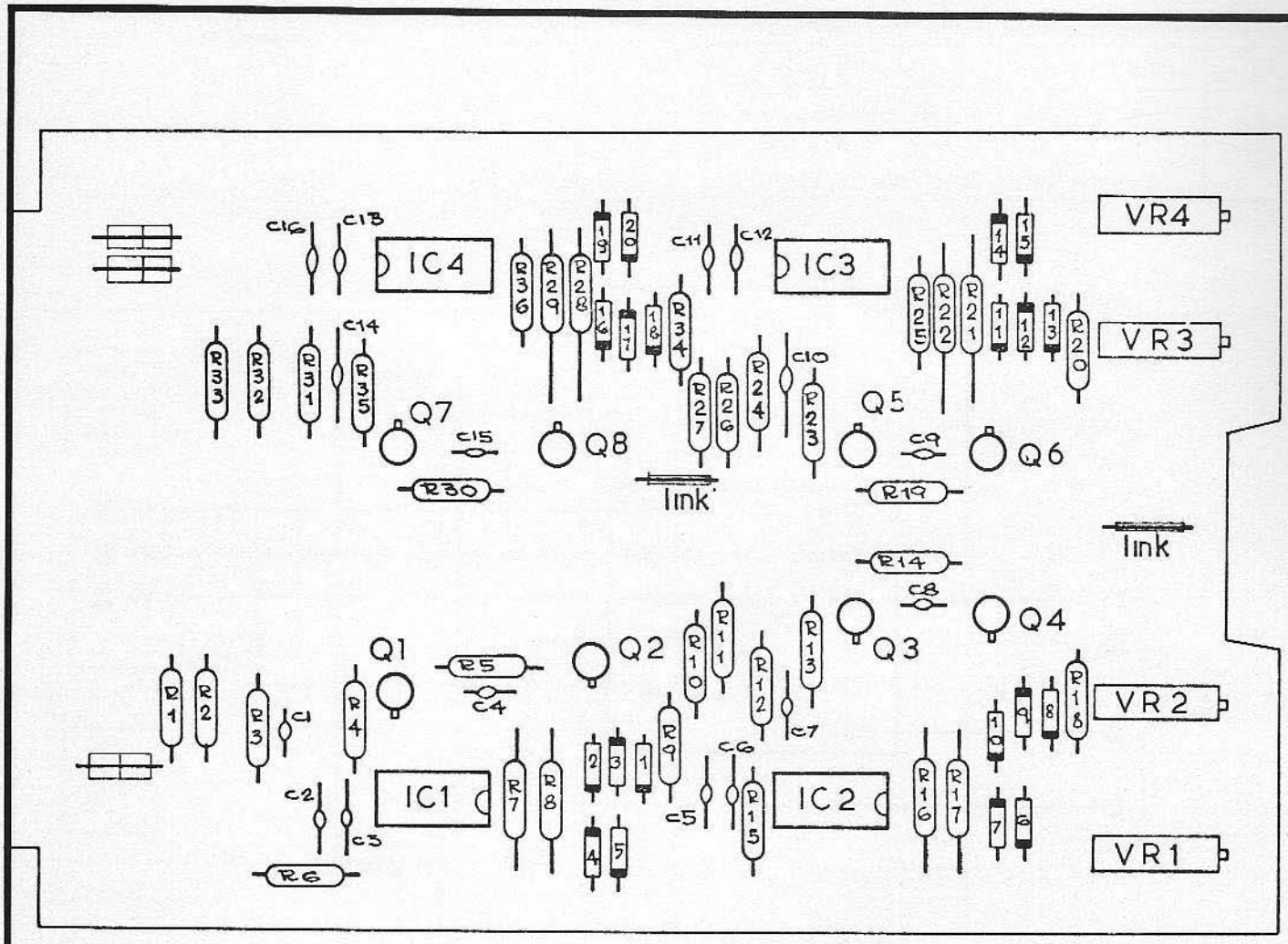


LEGEND:

5 Pin Nº on edge connector

◎ 4mm socket on front panel

ELECTRONIC ASSOCIATES PTY. LTD.			
TITLE: QUAD COMPARATOR CIRCUIT DIAGRAM			
NO. 180-59A			
PROJECT EAI-180			
DRAWN M.P.	DATE 2.8.72	DESIGNER G.F.G.	SHEET NO.



DESCRIPTION	CIRCUIT REF.
OP AMP IC	IC4-1
RESISTORS 1K	R1,2,9,10,11,18,20, 26,27,34,32,33;
RESISTORS 470	R3,12,24,31;
RESISTORS 6.8K	R4,13,23,35;
RESISTORS 8.2K	R14,19,5,30;
RESISTORS 47K	R6,15,25,36;
RESISTORS 100K	R7,8,16,17,21,22, 28,29:
CAPACITORS .047 UF	C2,3,5,6,11,12,13,16;
CAPACITORS 300 PF	C1,4,7,8,9,10,15,14;
DIODES	D1-18;
POTS 10K	VR1-4.

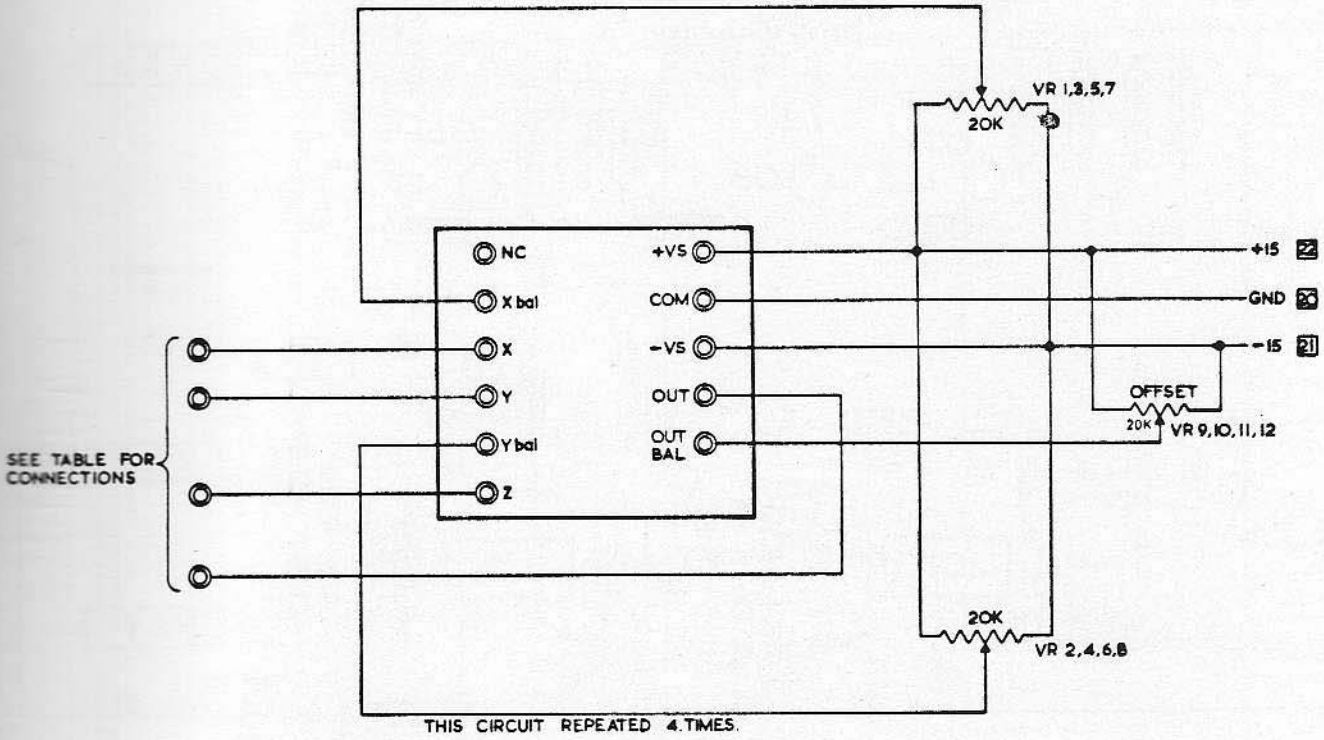
ELECTRONIC ASSOCIATES PTY. LTD.

TITLE: QUAD. COMPARATOR

NO.: 180-59D

PROJECT: EAI-180

DRAWN	DATE	DESIGNER	SHEET NO.
M.P.	16.8.72	G.F.G.	



SOCKET PIN N°'S

	Xin	Yin	Zin	Out
M1	4	6	5	7
M2	8	10	9	11
M3	12	14	13	15
M4	16	18	17	19

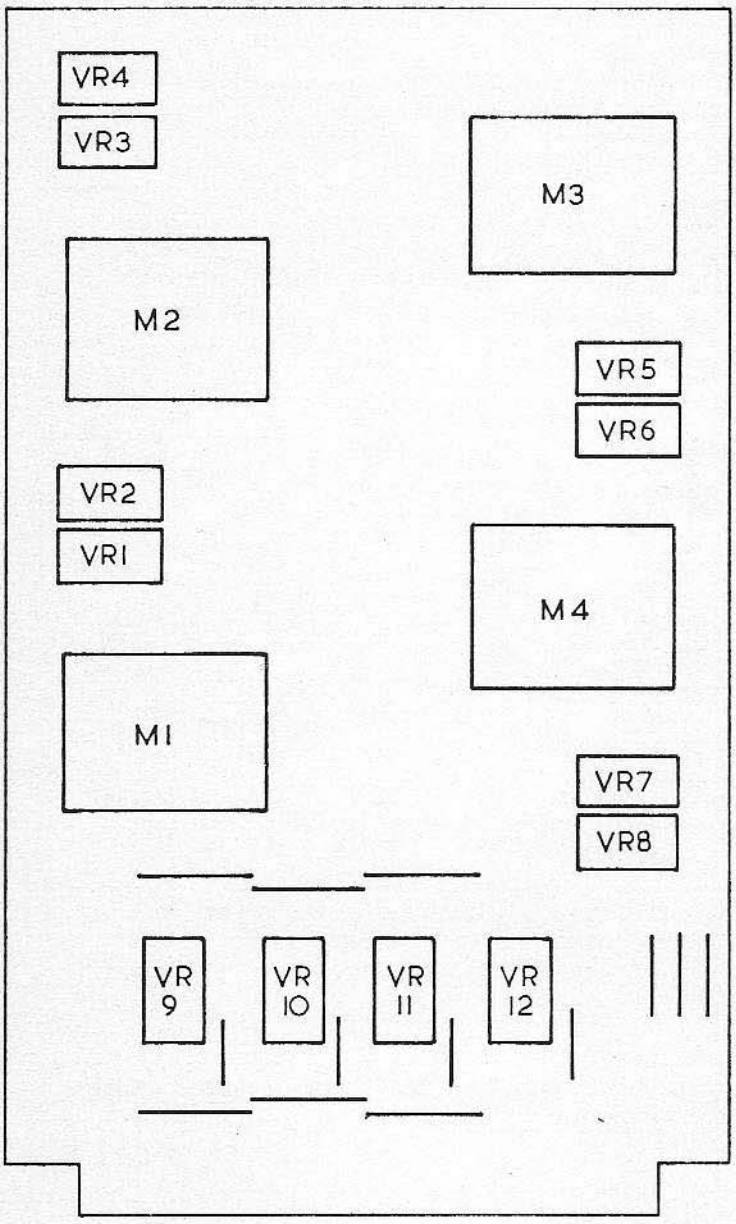
LEGEND:

◎ 4mm SOCKET ON FRONT PANEL

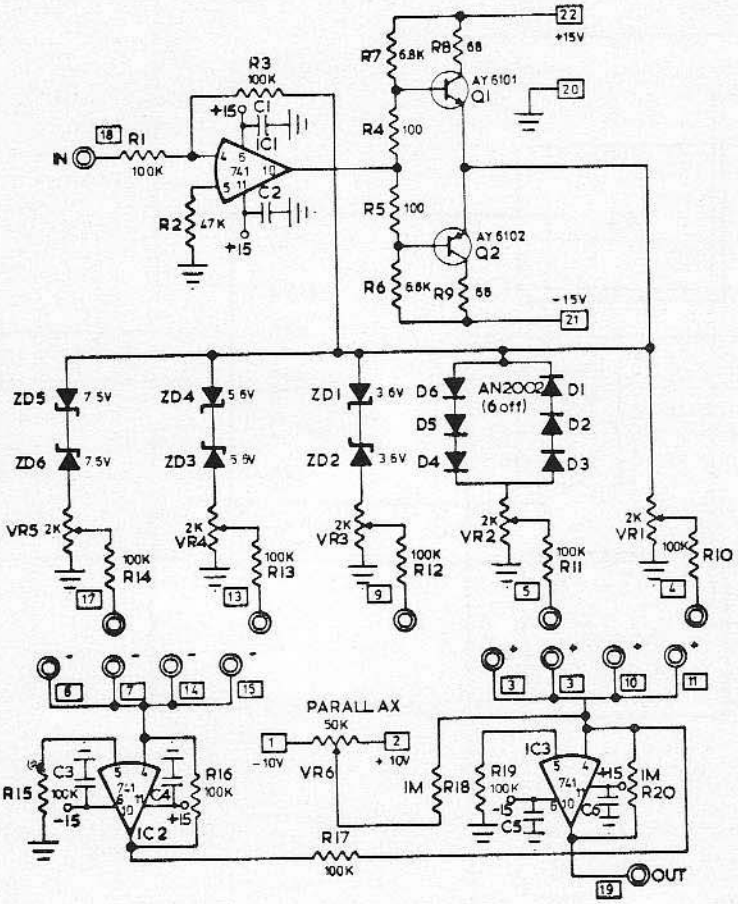
[5] Pin N° ON EDGE CONNECTOR

EAI ELECTRONIC ASSOCIATES PTY. LTD.			
TITLE: QUAD MULTIPLIER CIRCUIT DIAGRAM			
NO. 180-31A			
PROJECT EAI-180			
DRAWN M.P.	DATE 4.3.72.	DESIGNER G.F.G.	SHEET NO. 12A

DESCRIPTION	CIRCUIT REF.	QUAN
ANALOG MULTI-PLIER	M1,M2,M3, M4	4 MAX.
POTENTIOMETERS	VR1-VR12	12



EAI ELECTRONIC ASSOCIATES PTY. LTD.			
TITLE: QUAD MULTIPLIER MOD 180-31			
NO.: 180-31D			
PROJECT: EAI-180			
DRAWN: M.P.	DATE: 20.3.72.	DESIGNER: G.F.G.	SHEET NO.: 12B



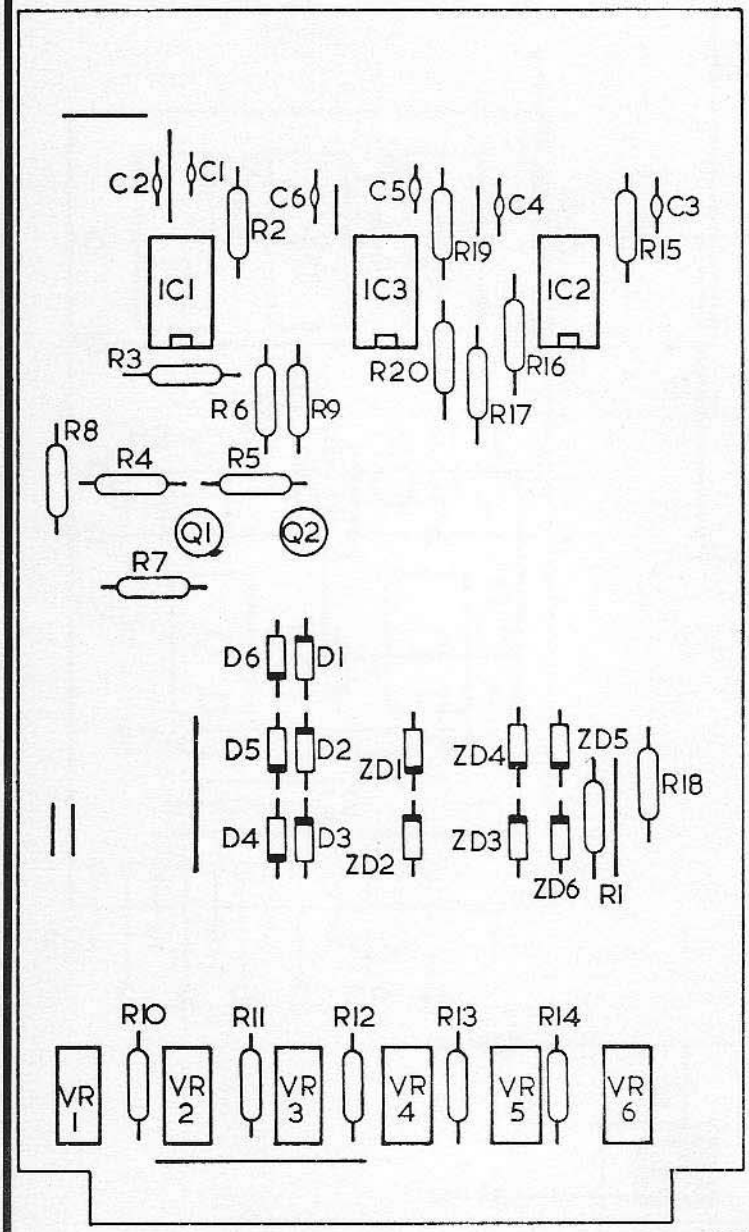
LEGEND:

SOCKET PIN Nº.

4mm SOCKET ON FRONT PANEL

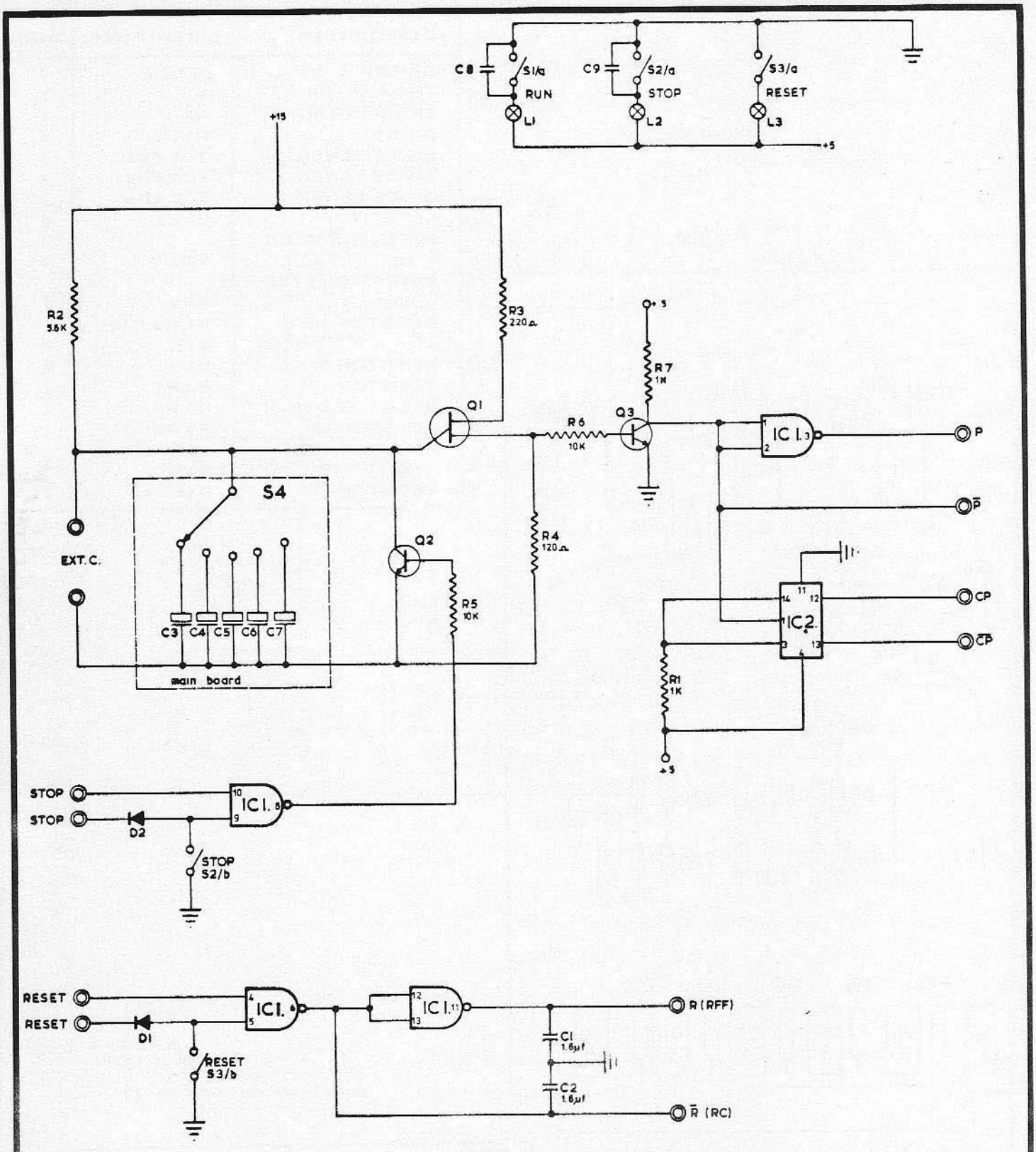
ELECTRONIC ASSOCIATES PTY. LTD.			
TITLE: EAI 180 DFG			
NO.: 180-28A			
PROJECT: EAI-180			
DRAWN: M.P.	DATE: G.F.G.	DESIGNER: 6.3.72.	SHEET NO.: 13A

DESCRIPTION	CIRCUIT REF.	QUAN
OP.AMP.IC	IC1,2,3	3
TRANSISTOR	Q1	1
TRANSISTOR	Q2	1
DIODE	D1-D6	6
DIODE ZENER	ZD1,ZD2	2
DIODE ZENER	ZD3,ZD4	2
DIODE ZENER	ZD5,ZD6	2
CAPACITOR	C1-C6	6
POTENTIOMETER 2K	VR1-V	5
POTENTIOMETER 50K	VR6	1
RESISTOR 100K	R1,R3,R16, R17	4
RESISTOR 47K	R2	2
RESISTOR 100	R4,R5	2
RESISTOR 6-8K	R6,R7	2
RESISTOR 68	R8,R9	2
RESISTOR 100K	R10-14,R15, R19	7
RESISTOR 1M	R18,R20	2



ELECTRONIC ASSOCIATES PTY. LTD.

TITLE: DFG MOD 180-28			
NO.: 180-28D			
PROJECT: EAI-180			
DRAWN: M.P.	DATE: 20.3.72.	DESIGNER: G.F.G.	SHEET NO.: 13B

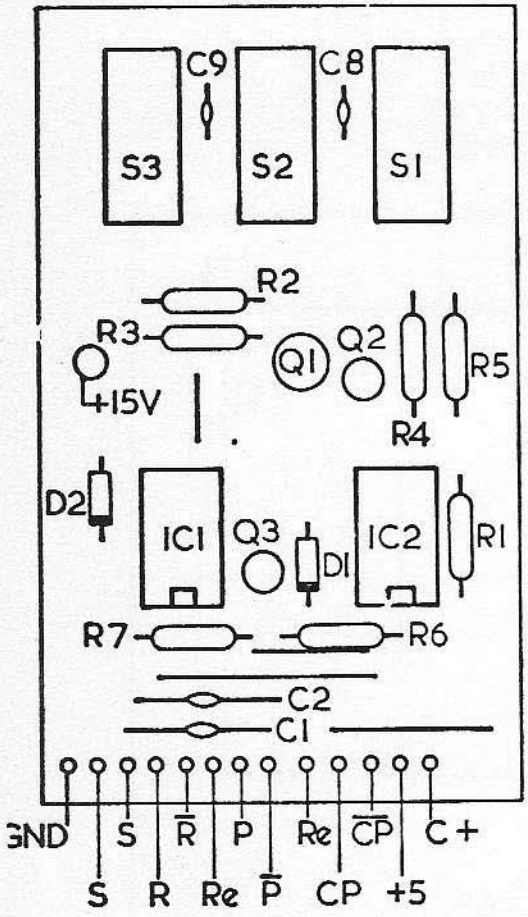


LEGEND:

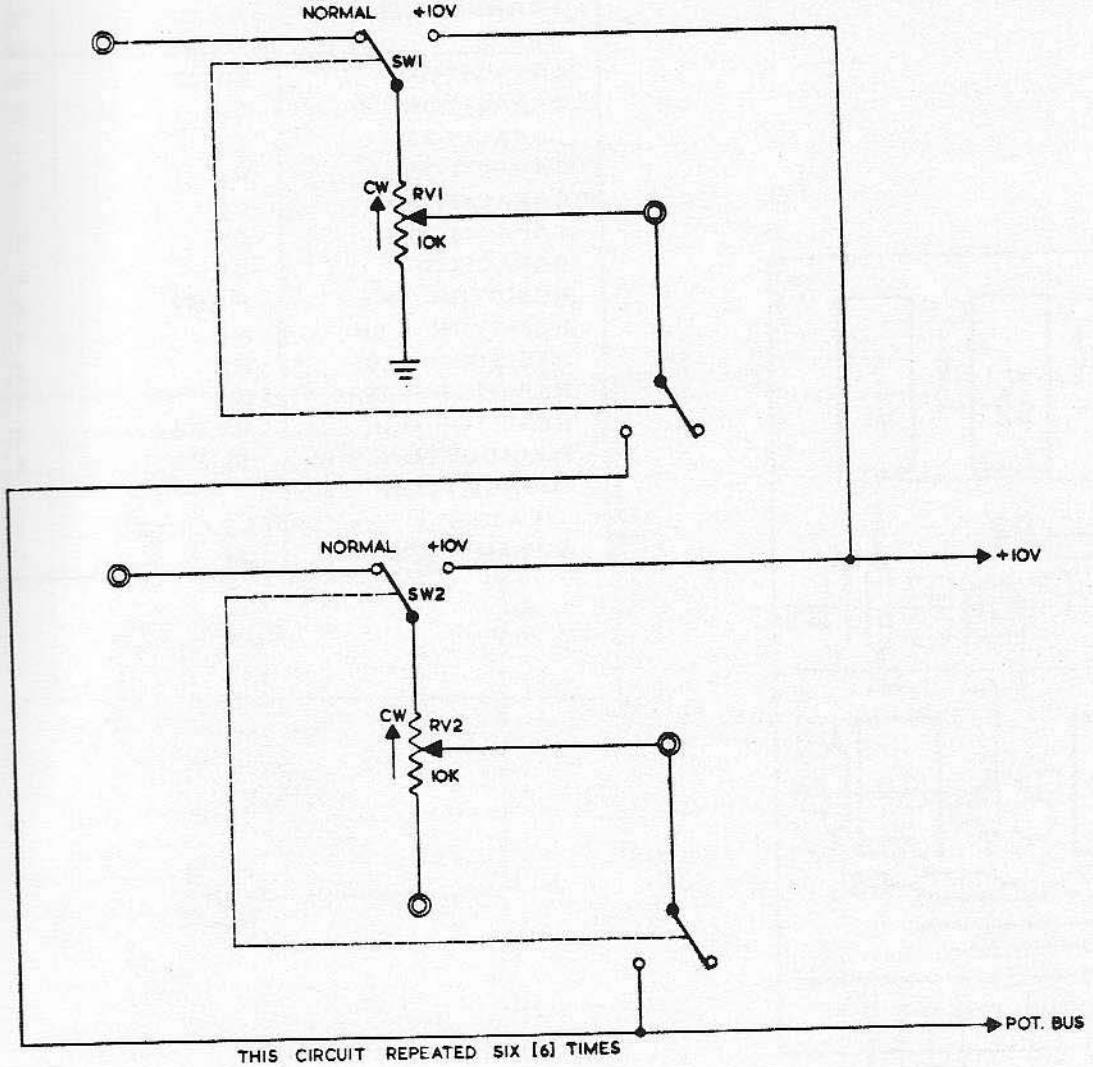
4mm socket on front panel

ELECTRONIC ASSOCIATES PTY. LTD.			
TITLE: DIGITAL CLOCK CIRCUIT DIAGRAM			
NO. 180-30A			
PROJECT EAI-180			
DRAWN M.P.	DATE 7.3.72.	DESIGNER G.F.G.	SHEET NO. 14A

DESCRIPTION	CIRCUIT REF.	QUAN
QUAD GATE IC	IC1	1
JK FF IC	IC2	1
TRANSISTOR U.J.	Q1	1
TRANSISTOR	Q2,Q3	2
DIODE	D1,D2	2
CAPACITOR	C1,C2	2
CAPACITOR	C3	1
CAPACITOR	C4	1
CAPACITOR	C5	1
CAPACITOR	C6	1
CAPACITOR	C7	1
CAPACITOR	C8,9	2
RESISTOR 1K	R1,R7	2
RESISTOR 5.6K	R2	1
RESISTOR 220	R3	1
RESISTOR 120	R4	1
RESISTOR 10K	R5,R6	2
PUSHBUTTON S/W	S1/2/3	1
PUSHBUTTON LAMPS	L1,L2,L3	3
ROTARY S/W	S4	1



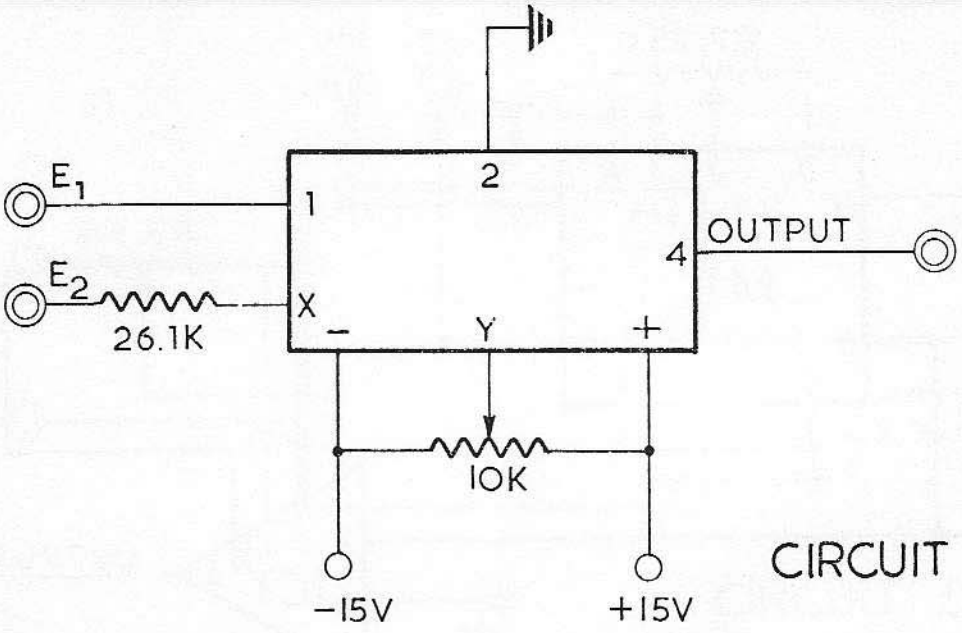
ELECTRONIC ASSOCIATES PTY. LTD.			
TITLE: DIGITAL CLOCK MOD. 180-30			
NO. 180-30D			
PROJECT EAI-180			
DRAWN M.P	DATE 18.3.72	DESIGNER G.F.G.	SHEET NO. 4



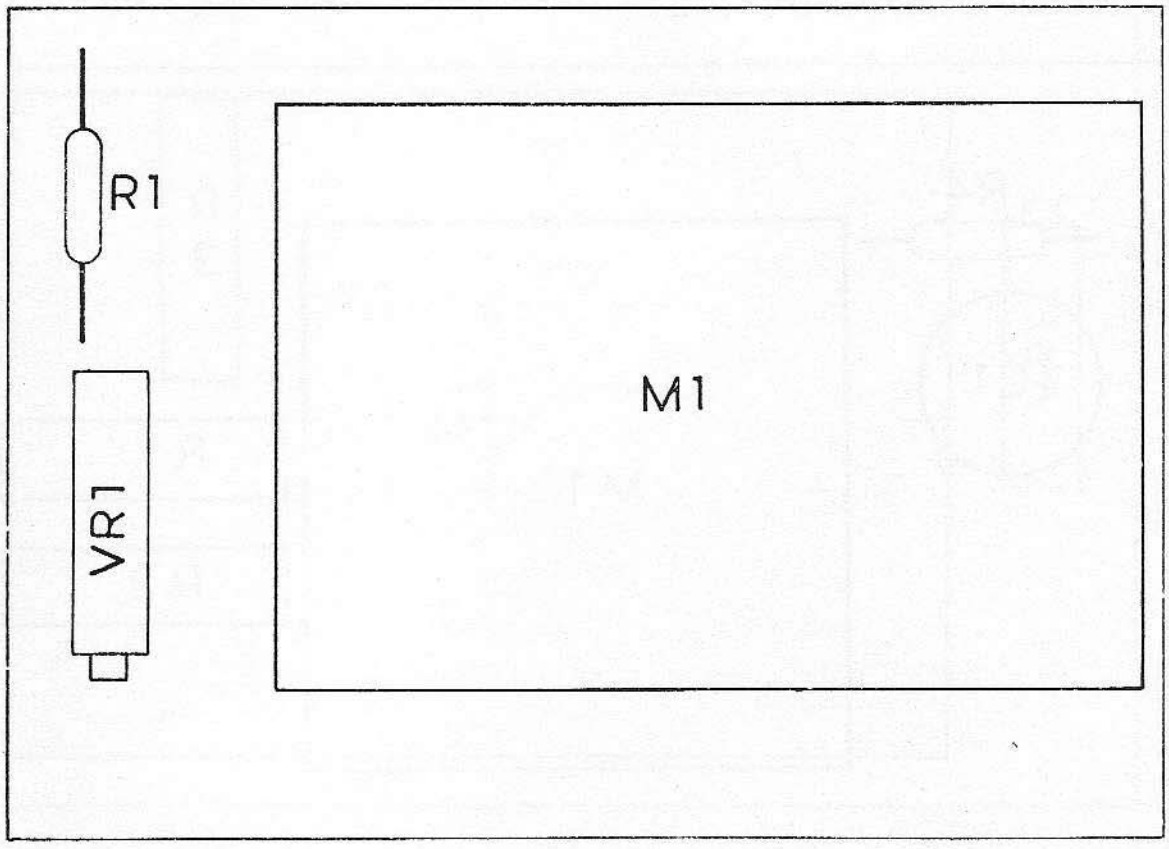
LEGEND

◎ 4mm socket on front panel

ELECTRONIC ASSOCIATES PTY. LTD.				
TITLE: POT BUS SWITCHING CIRCUIT1				
NO. 180-22A				
PROJECT EAI-180				
DRAWN M.P.	DATE 4.3.72.	DESIGNER G.F.G.	SHEET NO. 9	



CIRCUIT DIAGRAM



DESCRIPTION	CIRCUIT REF.	QUAN
RESISTOR 26.1K	R1	1
POTENTIOMETER 10K	VR1	1
SIN/COS MODULE	M1	1

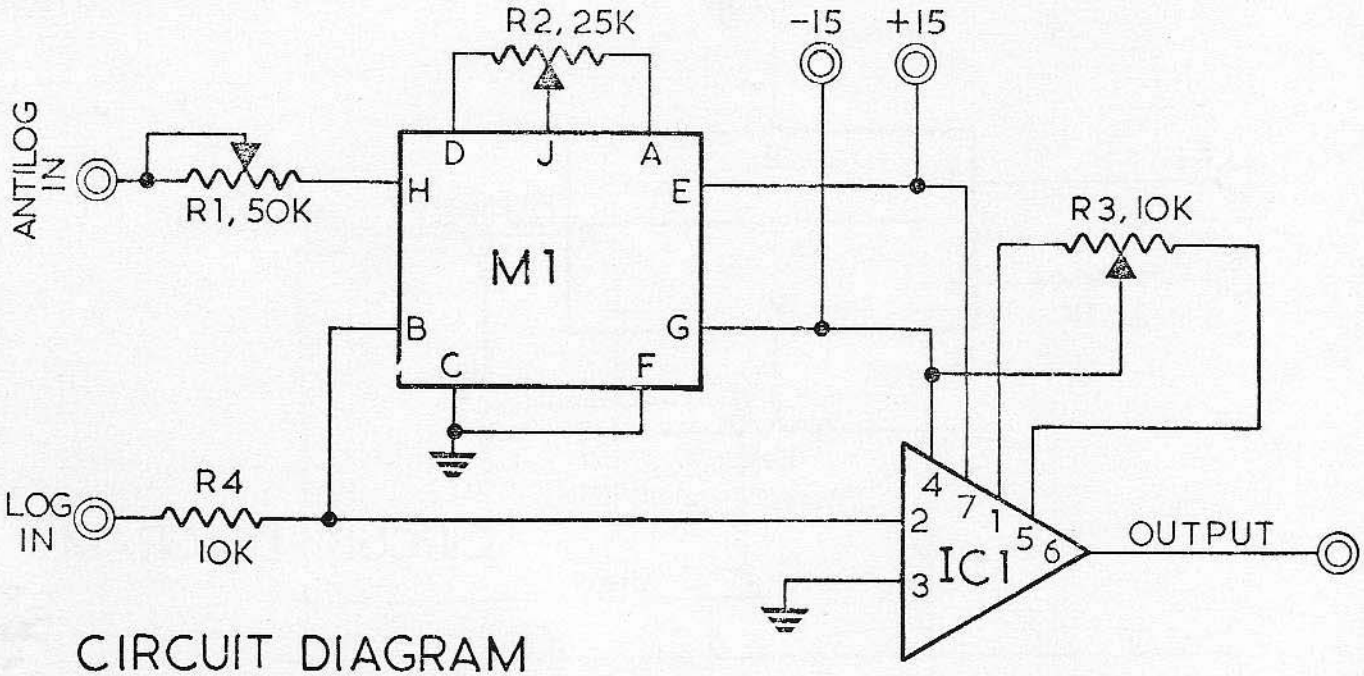
ELECTRONIC ASSOCIATES PTY. LTD.

TITLE: SIN/COS FUNCTION GENERATOR
CIRCUIT DIAGRAM & COMPONENT LAYOUT

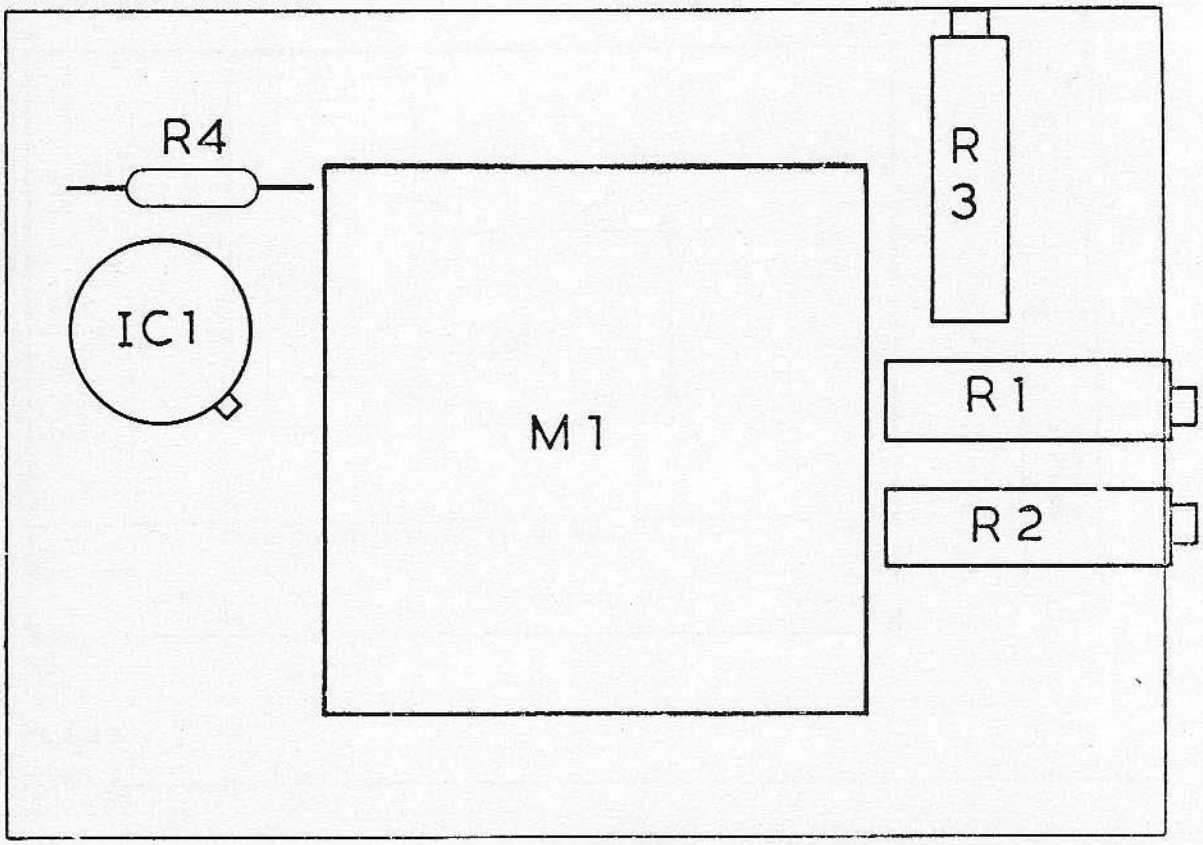
NO. 180-62 A & D

PROJECT EAI-180

DRAWN	DATE	DESIGNER	SHEET NO.
M.P.	24.5.72	G.F.G.	



CIRCUIT DIAGRAM



DESCRIPTION	CIRCUIT REF.	QUAN
POTENTIOMETER 50K	R1	1
POTENTIOMETER 25K	R2	1
POTENTIOMETER 10K	R3	1
IC AMPLIFIER	IC1	1
LOG MODULE	M1	1
RESISTOR 10K	R4	1

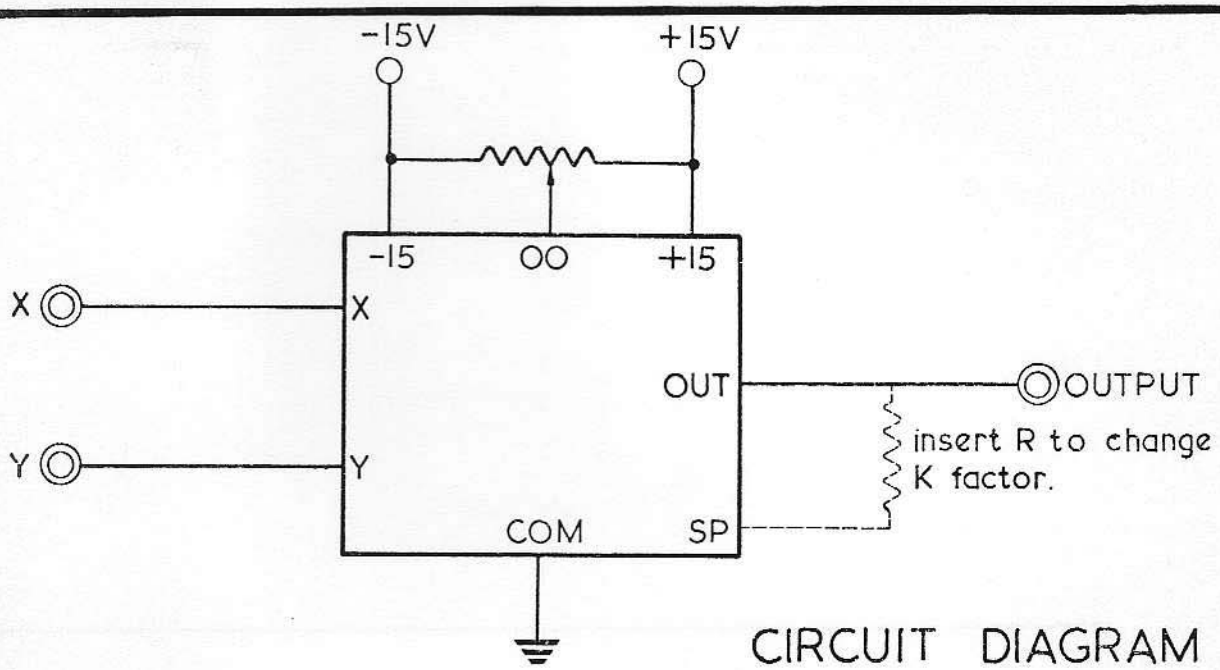
ELECTRONIC ASSOCIATES PTY. LTD.

TITLE
LOG/ANTILOG FUNCTION GENERATOR
CIRCUIT DIAGRAM & COMPONENT LAYOUT

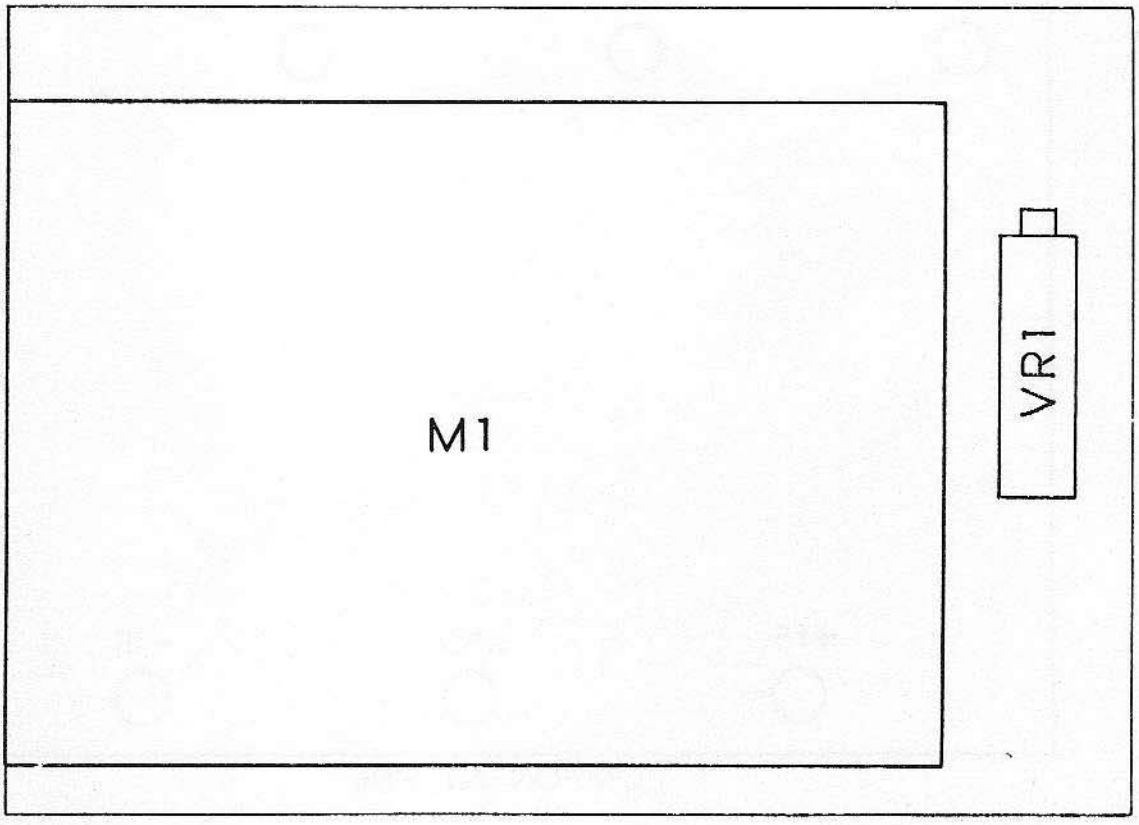
NO. 180-63 A & D

PROJECT EAI-180

DRAWN	DATE	DESIGNER	SHEET NO.
M.P.	25.8.72	G.F.G.	



CIRCUIT DIAGRAM



DESCRIPTION	CIRCUIT REF.	QUAN
POTENTIOMETER 50K	VR1	1
VECTOR MOD.	M1	1

ELECTRONIC ASSOCIATES PTY. LTD.

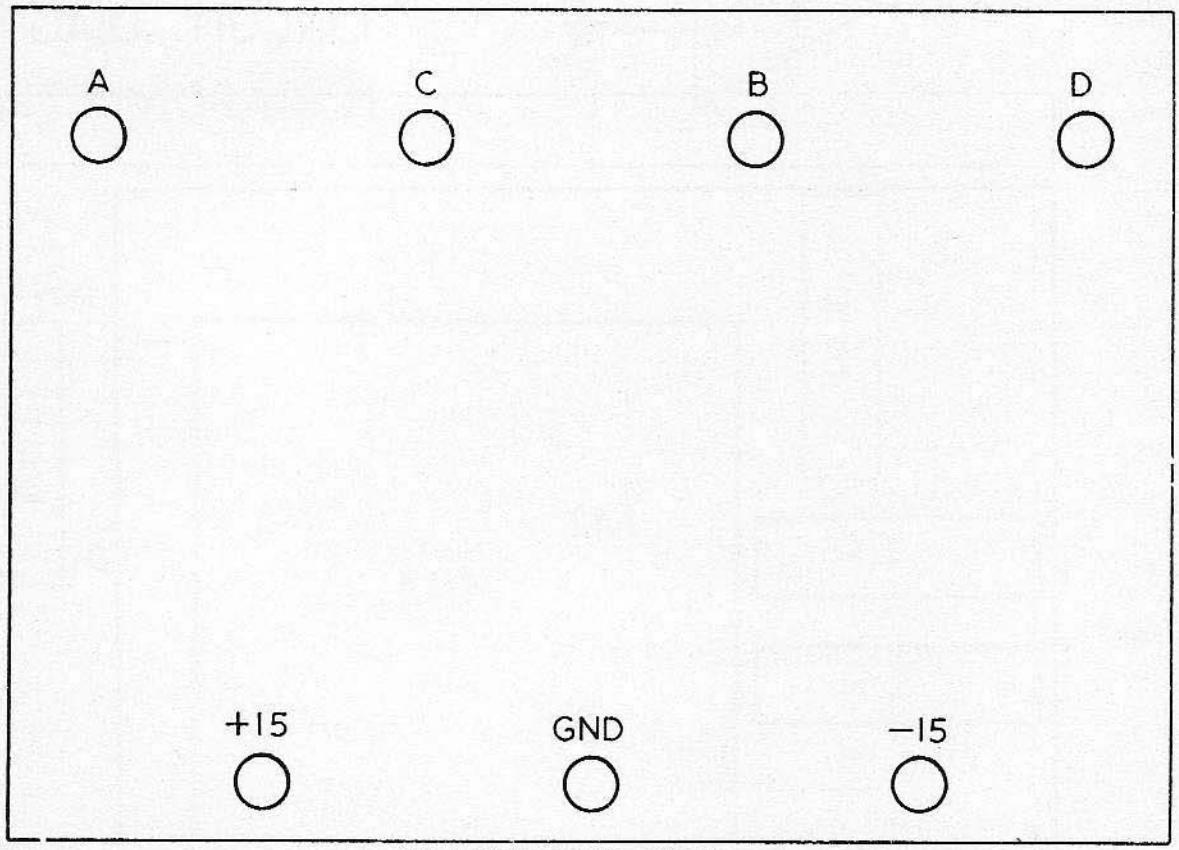
TITLE

VECTOR FUNCTION GENERATOR
CIRCUIT DIAGRAM & COMPONENT LAYOUT

NO. 180-64 A & D

PROJECT EAI-180

DRAWN	DATE	DESIGNER	SHEET NO.
M.P.	25.8.72	G.F.G.	



COMPONENT SIDE

ELECTRONIC ASSOCIATES PTY. LTD.			
TITLE: FREE FUNCTION GENERATOR CARD CONNECTIONS			
NO. 180-61 A & D			
PROJECT EAI-180			
DRAWN M.P.	DATE 25.8.72	DESIGNER G.F.G.	SHEET NO.

UNITED STATES AND CANADIAN OPERATIONS

LOCATION

United States

West Long Branch, New Jersey,
185 Monmouth Parkway,
West Long Branch, N.J. 07764.
TWX: 710-722-6597
TELEX: 132-443
CABLE: PACE W.Long Branch, N.J.
TELE: 201 229-1100

FACILITIES
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Computer Division
Computer Service Division
Principal Engineering and Manufacturing
Sales and Service
International Operations
Graphics and Instruments

Canada

Allen Crawford Associates Ltd.,
6427 Northam Drive,
Malton, Ontario, Canada
TELE: 416-678-1500.

FACILITIES
Sales and Service

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5101-10, 5201-5
TELEX: 851-87183
CABLE: PACE Burgess Hill

Sweden

EAI-Electronic Assiciates-AB,
Hagavagen 14,
171-53 Solna 3, Sweden.
TELE: 82.40.97
TELEX: Stockholm 854-10064.

FACILITIES
Sales and Service
Computation Centre

European Continent

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Brussels-B-1030, Belgium,
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TELEX: 846-21106
CABLE: PACEBELG Brussels

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75 737 Paris Cedex 15, France.
TELE: 577.08.13 (3 lines)
TELEX: PACEPAR 1 27610

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Franzstrasse 107,
5100 Aachen, West Germany.
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Sales and Service

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TELE: 439-7522 (4 lines)
CABLE: PACEAUS, Sydney.

Victorian Office
225 Park Street,
S. Melbourne,
Victoria, 3205, Australia.
TELE: 69-6108 (3 lines)

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Manufacturing

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EAI-Electronic Associates (Japan) Inc.
9th MORI Building,
1-3 Shiba-Atago-cho,
Minato-ku,
Tokyo, Japan 105.
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TELEX: 781-24285
CABLE: EAIJAPACE

FACILITIES
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CABLE: COASIN

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